CBCS SCHEME

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17EC53

Fifth Semester B.E. Degree Examination, June/July 2023
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the typical VLSI IC design flow with the help of flow chart. **(10 Marks)**

b. Explain the different levels of Abstract used for programming in verilog. **(10 Marks)**

OR

2 a. Why verilog HDL has evolved as popular HDL in digital circuit design. **(10 Marks)**

b. Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry Adder. (Hint : Full Adder (1-bit) is implemented using Half Adder as component) **(10 Marks)**

Module-2

3 a. List the different data types of verilog HDL. Explain data types with examples. **(12 Marks)**

b. What are the basic components of a module? Which components are mandatory? **(08 Marks)**

OR

4 a. What are the uses of $ display, $ monitor system tasks, explain with examples. **(08 Marks)**

b. Write verilog description of SR Latch. Also write stimulus code. **(04 Marks)**

c. Are these legal identifiers? If not write the reason.

i) System 1
ii) 5reg
iii) $latch
iv) exe#

(08 Marks)

Module-3

5 a. Write a verilog gate level of abstraction for 4 to 1 multiplexer. Write stimulus block. **(10 Marks)**

b. What would be the output of the following :

A = 3, B = 0, C = 4'b 1101, D = 4'b 1010

Z = 4'b 1XXZ, N = 4'b 1XXX

i) C – D
ii) A && B
iii) A < = D
iv) Z ! = = N
v) B + (D>>>1)

(10 Marks)

OR

6 a. Explain with example, different operators supported by verilog HDL. **(14 Marks)**

b. Write the verilog description of 4-bit carry look ahead adder at Data flow level abstraction, with a neat block diagram. **(06 Marks)**

Module-4

7 a. Explain combined part declaration and combined ANSI C-style port declaration with examples in verilog. **(04 Marks)**

b. Write 4-bit counter behavioral modeling program in verilog. **(08 Marks)**

c. Explain different loop statements in verilog. **(08 Marks)**

OR

8 a. Write a note with example for i) CASE ii) CASEX **(08 Marks)**

b. Design a negative edge – triggered D-flipflop (D_FF) with synchronous clear active high (D_FF clears only at a negative edge of clock when clear is high). Use behavioral statements only. Design a clock with a period of 10units. **(12 Marks)**

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Module-5

9 a. Explain the design tool flow followed in VLSI design with a neat flow diagram. **(10 Marks)**

b. List and explain the advantages and benefit of using VHDL. **(10 Marks)**

OR

10 a. Explain the relationship between a design entity and its declaration and architecture body in VHDL. **(10 Marks)**

b. Write a VHDL program for two (4bit data) comparator using behavioral description. **(10 Marks)**

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