CBCS SCHEME

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18EC34

# Third Semester B.E. Degree Examination, June/July 2023
## Digital System Design

Time: 3 hrs. Max. Marks: 100

***Note: Answer any FIVE full questions, choosing ONE full question from each module.***



### Module-1

1 a. A switching circuit has four inputs A, B, C and D and one output F. Inputs A and B represent the bits of number $N_1$, and C and D represent the bits of number $N_2$. The output is to be logic 1 only if the product $N_1 \times N_2$ is lesser than 2. Obtain the minterm and maxterm expressions in decimal notation for the output F. **(06 Marks)**

b. Simplify $f(A, B, C, D) = \sum m(1, 2, 3, 5, 6, 7, 9, 10, 11)$ using K-map to get the minimum SOP expression, as well as minimum POS expression. Among the two expressions, find out which one requires lesser number of gates for implementation? **(10 Marks)**

c. Convert $X = \bar{a}\,b + bc$ to canonical SOP form. **(04 Marks)**

**OR**

2 a. Four chairs A, B, C and D are placed in row. Each chair may be occupied (logic 1) or not occupied (logic 0). The output Y should go high only when adjacent chairs are occupied. Draw the truth table, obtain the maxterm expression and simplify the expression using K-map to get minimum POS expression. **(08 Marks)**

b. Simplify the function $f(A, B, C, D) = \sum m(9, 12, 13, 15) + \sum d(1, 4, 5, 7, 8, 11, 14)$ using QM technique. Identify the essential prime implicant, if any, and obtain at least two solutions. **(12 Marks)**

### Module-2

3 a. Give the truth table of full adder, derive the expressions for the outputs, and design a logic circuit for the same using minimum number of 2-input NAND gates only. **(10 Marks)**

b. Draw the block diagram of 4-bit look ahead carry adder. Derive the expressions for the carry outputs using propagate and generate inputs. **(10 Marks)**

**OR**

4 a. Implement full-subtractor circuit using one 3:8 decoder having active-low outputs. **(06 Marks)**

b. Implement the Boolean function $f(w, x, y, z) = \sum m(3, 5, 6, 8, 11, 13, 14, 15)$ using one 4 to 1 multiplexer and additional gates. Connect w and x inputs to select lines. **(06 Marks)**

c. Explain what is FPGA? Show how a 6-varibale function can be implemented using 4-input function generators and additional hardware and implemented as FPGA. **(08 Marks)**

### Module-3

5 a. Show how an SR latch can be used for switch debouncing. Explain with waveforms. **(06 Marks)**

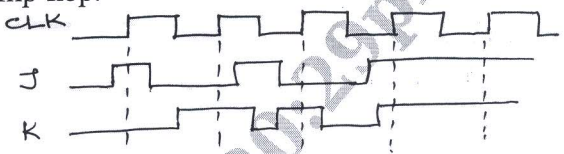
b. Bring out the differences between gated SR latch and master-slave SR flip-flop. Draw the circuits of both. **(06 Marks)**

c. Draw the block diagram of 3-bit bidirectional shift register capable of serial and parallel load and explain its operation. **(08 Marks)**

**OR**

6 a. Draw the Q and $\overline{Q}$ output waveforms if the waveforms given in Fig.Q.6(a) is fed to a positive edge-triggered JK flip flop. **(04 Marks)**

Fig.Q.6(a)




b. Using K-map simplification, obtain the characteristic equations of SR, JK and T flip-flops, and hence construct SR, JK and T flip flops using edge-triggered D flip flop. **(10 Marks)**

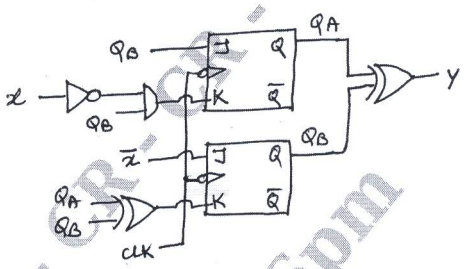
c. Construct a ripple counter that counts from 111 to 000 and repeats, using negative edge-triggered toggle flip-flops. Draw the waveforms showing one complete count cycle. **(06 Marks)**

## Module-4

7 a. Design a synchronous counter using JK flip flops, having the count sequence: 0, 1, 3, 5, 7 and repeats. The counter should be self-correcting if in case it goes into an unused state. **(12 Marks)**

b. Construct the transition table, state table and state diagram for the sequential circuit shown in Fig.Q.7(b). **(08 Marks)**

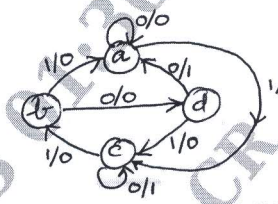
Fig.Q.7(b)




**OR**

8 a. Design a sequential circuit using JK flip flops for the state diagram shown in Fig.Q.8(a). **(12 Marks)**

Fig.Q.8(a)




b. With block diagrams, explain what are Moore and Mealy models of sequential circuits. Explain with one simple example each. What difference do you notice in drawing the state diagrams for both the models? **(08 Marks)**



## Module-5

9 a. Design a Mealy sequential circuit with one input and one output, using D flip flops, to detect the sequence 10110 with overlap. **(14 Marks)**

b. Draw the block diagram of a serial adder capable of adding two 4-bit numbers. Illustrate its working with an example. **(06 Marks)**

**OR**

10 a. Obtain the state diagram, state table and reduced state table for a 4-bit BCD to excess-3 sequential circuit with one input and one output. **(12 Marks)**

b. Draw the block diagram of a serial multiplier that can multiply two 4-bit unsigned numbers. Illustrate by multiplying the numbers 1011 and 1101. **(08 Marks)**

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