CBCS SCHEME

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15EC33

Third Semester B.E. Degree Examination, June/July 2023
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. A digital system has three inputs A, B and C and one output Y. If A = B then Y is complement of C. If A ≠ B then Y is same as C. Draw the truth table of the system and express the output as sum of minterms and product of maxterms in decimal notation. **(06 Marks)**

b. Simplify the function $F(w, x, y, z) = \pi(3, 4, 6, 7, 11, 12, 13, 14, 15)$ using K-map and write the simplified expression as product of sums. **(05 Marks)**

c. Simplify the function $F(a, b, c, d) = \Sigma(3, 5, 7, 10, 11, 13, 14) + \Sigma_d(1, 9, 12, 15)$ using K-map and write the simplified expression as sum of products. **(05 Marks)**

OR

2 a. Simplify $F(a, b, c, d) = \Sigma_m(0, 1, 5, 6, 8, 9, 11, 13) + \Sigma_d(7, 10\ 12)$ using QM method. Identify the essential prime implicants and write the final expression. **(10 Marks)**

b. Realize $F = \bar{x}z + x\bar{z} + y$ using only NAND gates, and then using only NOR gates. **(06 Marks)**

Module-2

3 a. Design a full subtractor and implement the same using two half subtractors and an additional gate. **(08 Marks)**

b. Explain 4-bit carry look-ahead adder with block diagram and logic diagrams. **(08 Marks)**

OR

4 a. Design a 2-bit magnitude comparator to compare two 2-bit numbers, and realize the same using any logic gates. **(08 Marks)**

b. Give the truth table of full-adder, and implement the same using one 3 : 8 decoder with active-two outputs and additional gates. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain the operation of negative edge triggered master slave D flip-flop. Draw sample waveforms to support the exploration. **(06 Marks)**

b. With diagram and heat waveforms, explain how SR latch can be used as switch debouncer. **(06 Marks)**

c. With a neat diagram, show how JK flip-flop can be converted into D flip-flop and T flip-flop. **(04 Marks)**

OR

6 a. Draw Q and $\bar{A}$ output waveforms of a negative edge triggered JK flip-flop if the inputs are as indicated in Fig.Q6(a). **(04 Marks)**

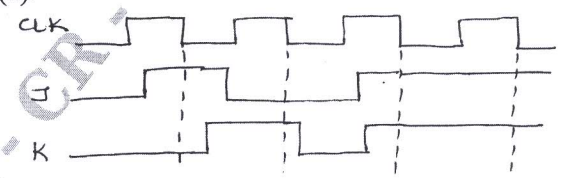

Fig.Q6(a)

b. Using K-map simplification, obtain the characteristics equations of SR, JK and T flip-flops. **(06 Marks)**

c. Draw the circuit of positive edge triggered D-flip-flop using NAND gates and explain its operation. **(06 Marks)**

Module-4

7 a. Construct 3-bit ripple up counter using negative edge-triggered T-flip-flops, and draw the waveforms showing all the states. **(08 Marks)**

b. Construct 3-bit parallel-in serial-out shift register using positive edge- triggered D-flip-flops and example the operation. **(08 Marks)**

OR

8 a. Design a synchronous counter having the count sequence 0, 2, 3, 5, 6 using D-flip-flops. **(08 Marks)**

b. Design mod-6 ripple counter using negative edge triggered JK flip-flops having clear inputs. Draw the waveform showing all the states. **(08 Marks)**

Module-5

9 a. With block diagrams, explain the Moore and Mealy models of synchronous sequential circuits. **(08 Marks)**

b. Analyze the sequential circuit given in Fig.Q9(b) and obtain the transition and state tables.

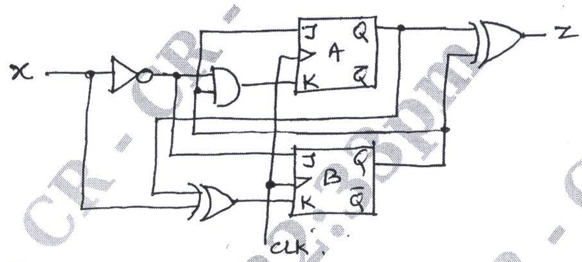

Fig.Q9(b) **(08 Marks)**

OR

10 a. Design a sequential circuit for the state diagram shown in Fig.Q10(a) using D flip-flops. Assume $S_1 = 00$, $S_2 = 01$, $S_3 = 10$.

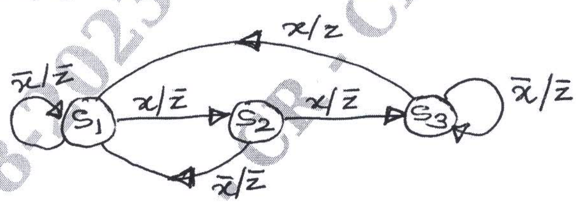

Fig.Q10(a) **(12 Marks)**

b. Give the application tables or excitation tables of D, T, SR and JK T-flip-flops. **(04 Marks)**

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