CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, Jan./Feb. 2023

Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

SOLUTION

Sub: Analog and Digital Electronics
Sub Code: 18CS33
Session: July 2022/ Jan 2023
Branch: CSE

Course Instructor:
Prof. Pratham Majumder
&
Prof. Paramita Mitra

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpra

Module-1

1 a. Explain the construction and working principle of LED. **(05 Marks)**

b. List the types of transistor biasing. Explain Fixed Bias Circuit with necessary analysis. **(06 Marks)**

c. Explain the operation of astable multivibrator using IC555 and derive the expression for time period, frequency and duty cycle. **(09 Marks)**

OR

2 a. Explain the operation of peak detector circuit with neat diagram. **(05 Marks)**

b. List and explain the performance parameters of regulated power supply. **(06 Marks)**

c. Explain the 3 bit flush type ADC with necessary circuit and truth table. **(09 Marks)**

Module-2

3 a. Find the minimum sum of products using K-map and identify prime implicants.
$f(a,b,c,d) = \sum m(0,2,6,10,11,12,13) + d(3,4,5,14,15)$ **(06 Marks)**

b. Find the minimum SOP and POS using K-map.
$f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$ **(08 Marks)**

c. List the steps for Petrick's method. **(06 Marks)**

OR

4 a. Find all the prime implicants using Quine Mc Cluskey method. Verify the result using K-map.
$f(w,x,y,z) = \sum m(7,9,12,13,14,15) + d(4,11)$ **(12 Marks)**

b. Using Prime implication chart, find all the minimum SOP of the function using Quine McCluskey method.
$f(a,b,c,d) = \sum m(0,1,2,3,10,11,12,13,14,15)$ **(08 Marks)**

Module-3

5 a. Realize the function using only two input NAND gate and inverters.
$f_1 = \sum m(0,2,3,4,5)$, $f_2 = \sum m(0,2,3,4,7)$, $f_3 = \sum m(1,2,6,7)$ **(06 Marks)**

b. Draw the timing diagram of the circuit. Assume propagation delay of each gate is 20 ns. **(05 Marks)**

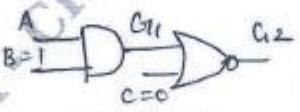


Fig. Q5 (b) – (i)

Fig. Q5 (b) – (ii)

c. List the types of hazards. Explain how static 1 hazard can be detected and removed with suitable example. **(09 Marks)**

OR

6	a.	Write short notes on three state buffers.	(06 Marks)
	b.	Design 7-segment decoder using PLA.	(06 Marks)
	c.	Construct 8 : 1 mux using only 2 : 1 mux.	(08 Marks)

Module-4

7	a.	Given that A = "00101101" and B = "10011". Determine the value of F F<=not B & "0111" or A&"1" and "1"&A	(04 Marks)
	b.	Write the complete VHDL code for 4 bit binary adder.	(08 Marks)
	c.	Explain how the VHDL code can be compiled simulated and synthesized with example.	(08 Marks)

OR

8	a.	Explain T Flip Flop with truth table.	(07 Marks)
	b.	Explain Master-Slave JK flip flop with neat diagram.	(08 Marks)
	c.	Write short notes on switch debouncing with an SR Latch.	(05 Marks)

Module-5

9	a.	Explain 8 bit serial in serial out shift register.	(10 Marks)
	b.	Explain n bit parallel adder with accumulator.	(10 Marks)

OR

10	a.	Design and explain mod 8 synchronous counter using JK flip flop.	(10 Marks)
	b.	Explain how moore transition and states can be constructed with examples.	(10 Marks)

* * * * *

Answers

Q1

Photodiode: A photodiode is a light detector semiconductor device that converts light energy into electric current or voltage which depends upon the mode of operation.

Construction

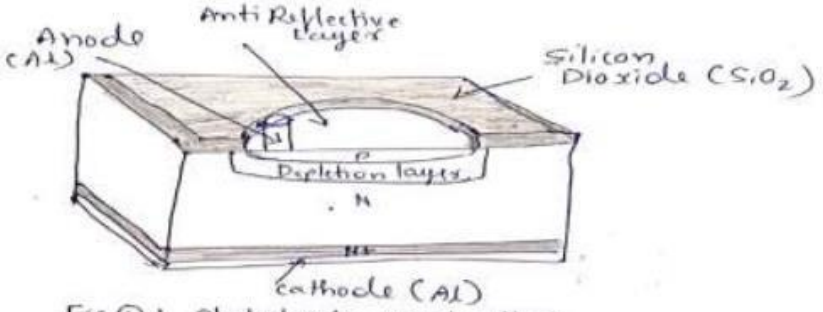


Fig ①: Photodiode construction

→ The typical construction of a photodiode is shown in fig ①.

→ Here construction technique called ion implantation is used where the surface of a layer of N-type is bombarded with P-type silicon ions to produce a P-type layer about 1μm thick.

→ During formation of the diode, excess electrons move from n-type to p-type & excess holes move from p-type to n-type this process is called diffusion, resulting in creation of a depletion layer as shown in above fig ①

Astable multivibrator using 555:

→ Astable multivibrator doesn't have any stable state. it is also called as free running multivibrator.

operation :

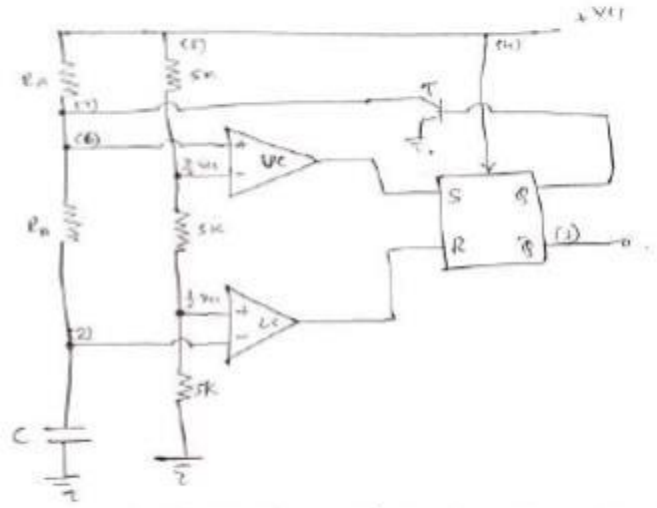


Fig ① Astable multivibrator using IC-555

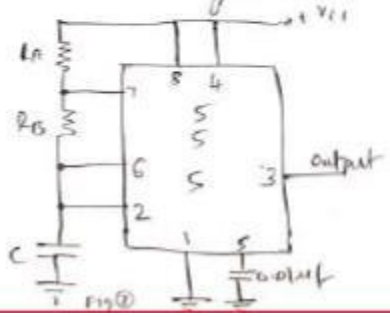
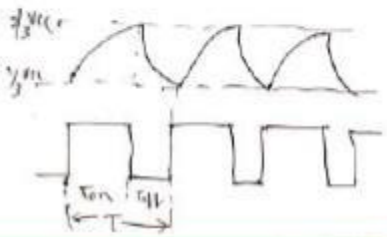


Fig ②



→ At $t=0$, the voltage on the capacitor $V_c = 0$, the sc voltage is applied to both trigger point of low comparator and upper comparator.

→ As $V_c = 0$, which is less than $\frac{1}{3}V_{cc}$, the output of lower comparator goes high ($\bar{Q} = 1$) and $Q =$

→ The capacitor starts charging through R_A & when V_c reaches $\frac{2}{3}V_{cc}$, the upper compar output goes high & it will set the SR FF i. $Q = 1$, $\bar{Q} = 0$.

→ The capacitor starts discharging through R_B transistor T. when $V_c = \frac{1}{3}V_{cc}$, the lower comparator output goes high.

→ This process of charging and discharging i continuous & hence circuit is called digital oscillator.

→ The on period T_{on} is given by

$$T_{on} = 0.693 (R_A + R_B) C$$

→ The discharging time T_{off} is

$$T_{off} = 0.693 R_B C$$

→ duty cycle is given by

$$D = \frac{\text{on time}}{\text{Total time}} = \frac{T_{on}}{T}$$

$$\therefore \% D = \frac{T_{on}}{T} \times 100$$

$$= \frac{0.693 (R_A + R_B) C}{0.693 (R_A + 2R_B) C} \times 100$$

$$\% D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

Photodiode: A photodiode is a light detector semiconductor device that converts light energy into electric current or voltage which depends upon the mode of operation.

Construction

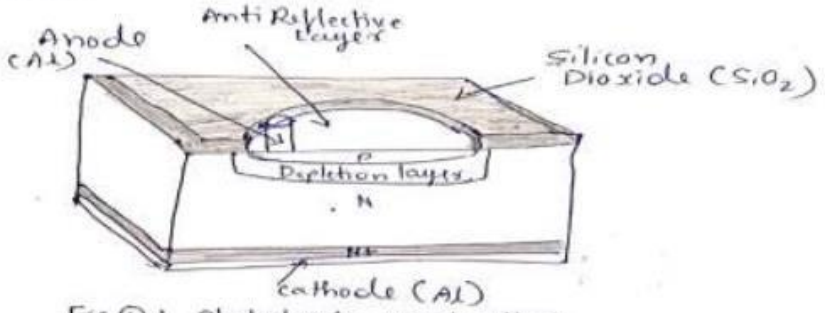


Fig ①: Photodiode construction

→ The typical construction of a photodiode is shown in fig ①.

→ Here construction technique called ion implantation is used where the surface of a layer of N-type is bombarded with P-type silicon ions to produce a P-type layer about 1μm thick.

→ During formation of the diode, excess electrons move from n-type to p-type & excess holes move from p-type to n-type this process is called diffusion, resulting in creation of a depletion layer as shown in above fig ①

Q2

Peak detectors

→ Peak detector detects the peak values of non-sinusoidal wave. Peak detector detects and holds the most positive value attained by the input signal.

→ Fig ① shows peak detector circuit.

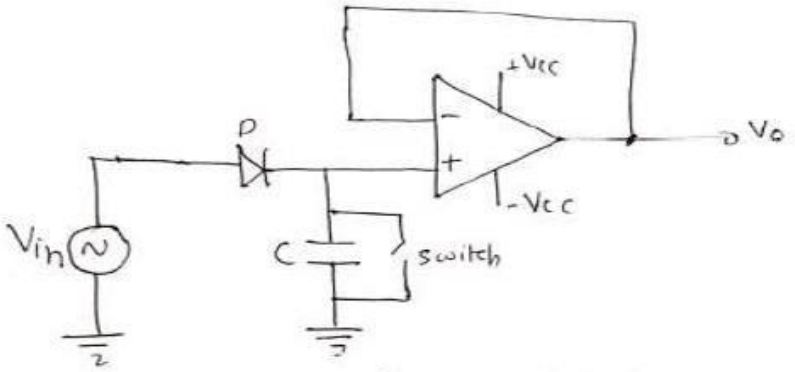


Fig ① peak detector circuit.

→ During positive half cycle of the input, diode is forward biased and capacitor C charges to peak value of input as shown in Fig ②.

Q3

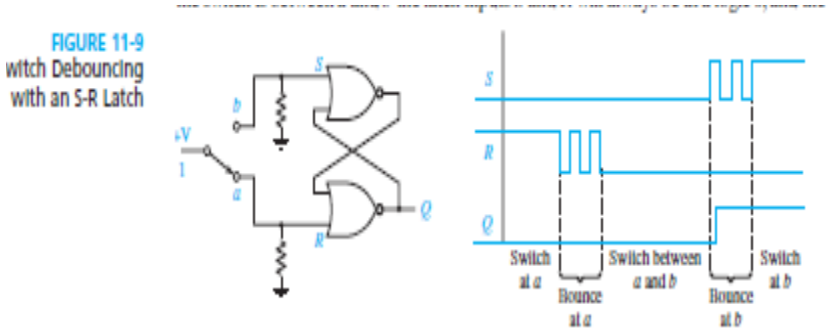
4-bit parallel Adder

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY FA IS
PORT(A,B,CIN:IN STD_LOGIC;SUM,COUT:OUT STD_LOGIC);
END FA;

ARCHITECTURE BEHV OF FA IS
BEGIN
SUM<=A XOR B XOR CIN;
COUT<=(A AND B) OR (B AND CIN) OR (A AND CIN);
END BEHV;

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY ADDER_4BIT IS
PORT(A,B:IN STD_LOGIC_VECTOR(3 DOWNTO 0);S:OUT STD_LOGIC_VECTOR(3 DOWNTO 0);C:OUT STD_LOGIC);
END ADDER_4BIT;

ARCHITECTURE BEHV OF ADDER_4BIT IS
SIGNAL TEMP:STD_LOGIC:='0';
SIGNAL CAR:STD_LOGIC_VECTOR(2 DOWNTO 0);
BEGIN
        FA1:ENTITY WORK.FA PORT MAP(A(0),B(0),TEMP,S(0),CAR(0));
```

```
        FA2:ENTITY WORK.FA PORT MAP(A(1),B(1),CAR(0),S(1),CAR(1));
        FA3:ENTITY WORK.FA PORT MAP(A(2),B(2),CAR(1),S(2),CAR(2));
        FA4:ENTITY WORK.FA PORT MAP(A(3),B(3),CAR(2),S(3),C);
END BEHV;
```

Q4

SR Latch – Switch Debouncing:



When a mechanical switch is opened or closed, the switch contacts tend to vibrate or bounce open and closed several times before settling down to their final position. This produces a noisy transition, and this noise can interfere with the proper operation of a logic circuit. This can be avoided by contacting to SR latch.

The input to the switch in Figure above is connected to a logic 1 (+V).The pull-down resistors connected to contacts *a* and *b* assure that when the switch is between *a* and *b* the latch inputs *S* and *R* will always be at a logic 0, and the latch output will not change state.

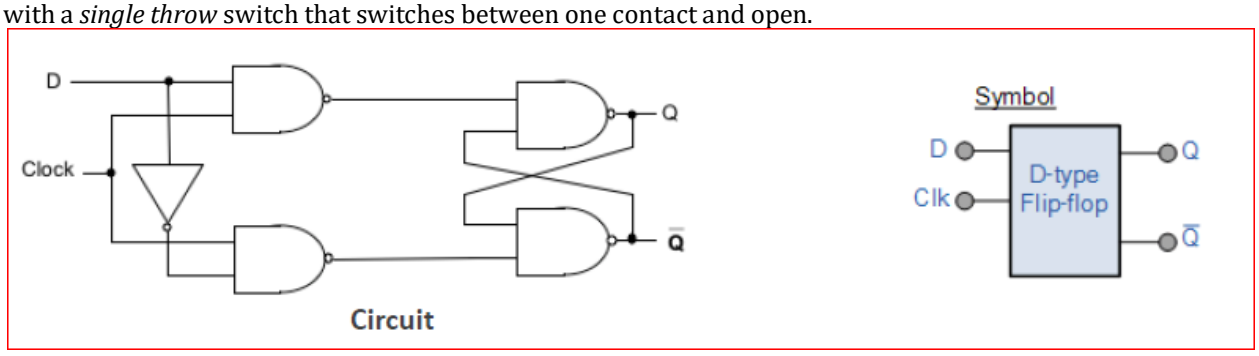
The timing diagram shows what happens when the switch is flipped from *a* to*b*.

As the switch leaves *a*, bounces occur at the *R* input; when the switch reaches *b*, bounces occur at the *S* input.

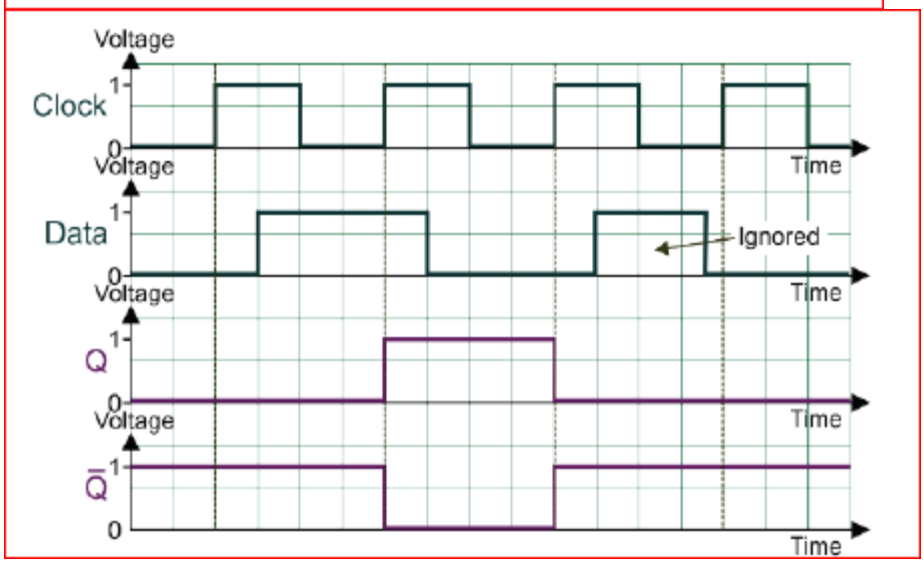
After the switch reaches *b*, the first time *S* becomes 1, after a short delay the latch switches to the *Q* =1 state and remains there.

Thus *Q* is free of all bounces even though the switch contacts bounce.

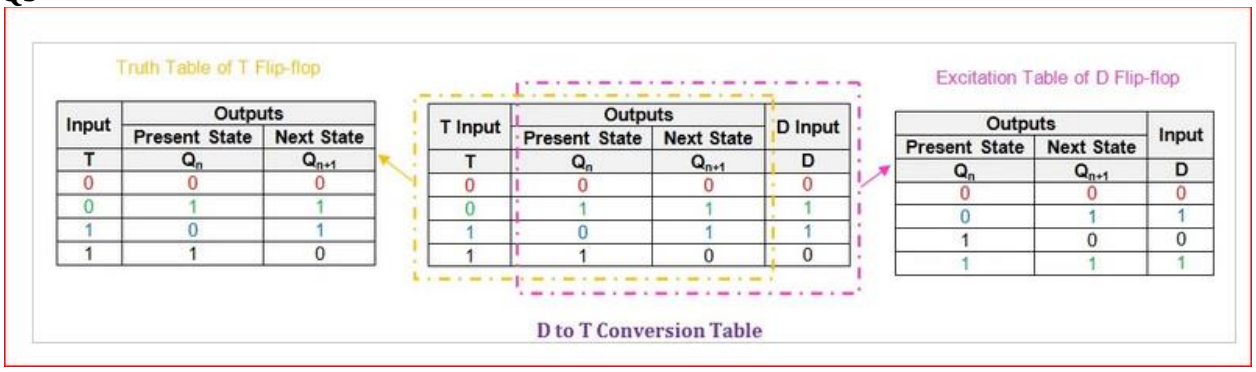
This debouncing scheme requires a *double throw* switch that switches between two contacts; it will not work with a *single throw* switch that switches between one contact and open.



CLK	D	Q	Status
0	X	Q_0	No change
↑	0	0	Reset
↑	1	1	Set



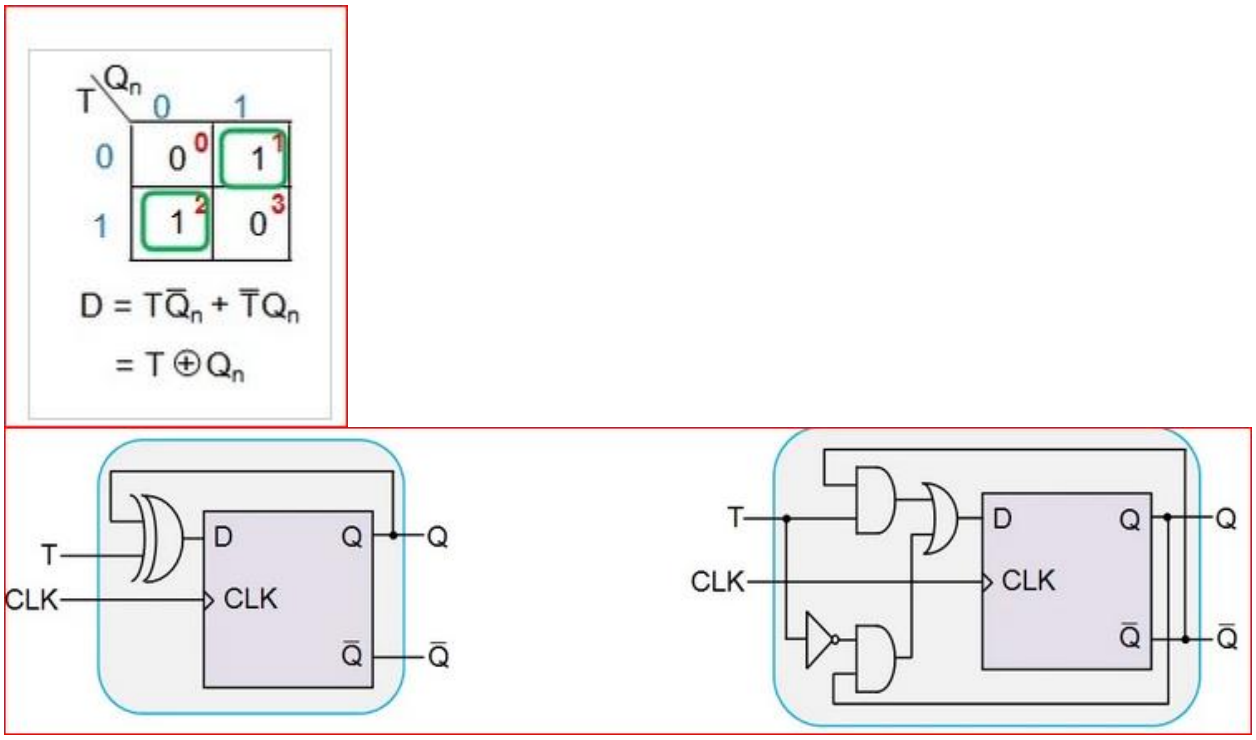
Q5



Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

T Input	Outputs		D Input
	Present State	Next State	
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

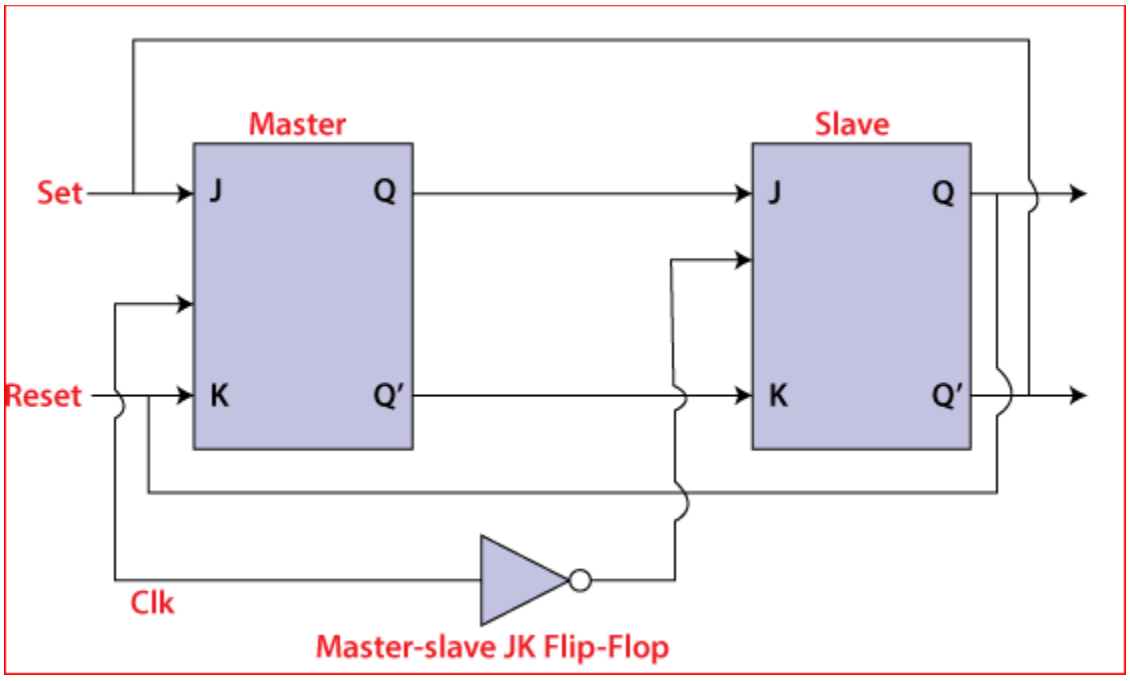
Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1



Master Slave JK F/F:
In "JK Flip Flop", when both the inputs and CLK set to 1 for a long time, then Q output toggle until the CLK is 1. Thus, the uncertain or unreliable output produces. This problem is referred to as a race-round condition in JK flip-flop and avoided by ensuring that the CLK set to 1 only for a very short time.

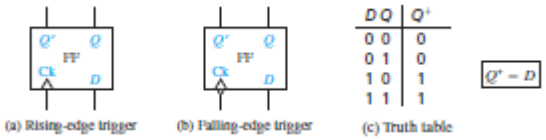
The master-slave flip flop is constructed by combining two JK flip flops. These flip flops are connected in a series configuration. In these two flip flops, the 1st flip flop work as "master", called the master flip flop, and the 2nd work as a "slave", called slave flip flop. The master-slave flip flop is designed in such a way that the output of the "master" flip flop is passed to both the inputs of the "slave" flip flop. The output of the "slave" flip flop is passed to inputs of the master flip flop.

In "master-slave flip flop", apart from these two flip flops, an inverter or NOT gate is also used. For passing the inverted clock pulse to the "slave" flip flop, the inverter is connected to the clock's pulse. In simple words, when CP set to false for "master", then CP is set to true for "slave", and when CP set to true for "master", then CP is set to false for "slave".



Q6 D flip-flop

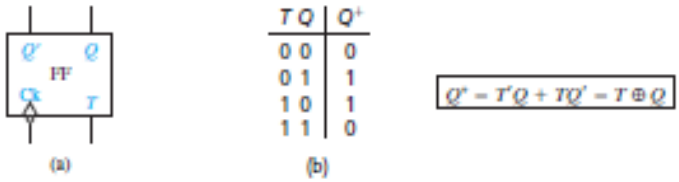
FIGURE 11-13
D Flip-Flops



Next state Q+ output 1 when D=1

(b) T flip-flop

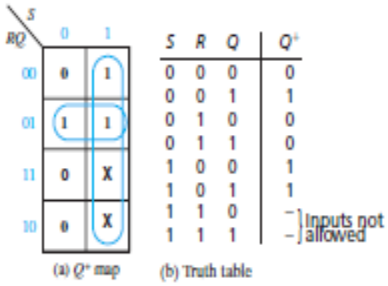
FIGURE 11-22
T Flip-Flop



Next state Q+ output 1 when T=1 and Q=0 or T=0 and Q=1

(c) S-R latch or flip-flop

FIGURE 11-8
Derivation of Q^+ for an S-R Latch

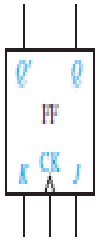


$Q^+ = S + R'Q \qquad (SR = 0)$

Q+ -next state Q –present state

Next state Q+ output 1 when S=1 or when R=0 and Q=1.
(d) J-K flip-flop

FIGURE 11-20
J-K Flip-Flop
(Q Changes on the Rising Edge)



(a) J-K flip-flop

J K Q	Q+
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	0

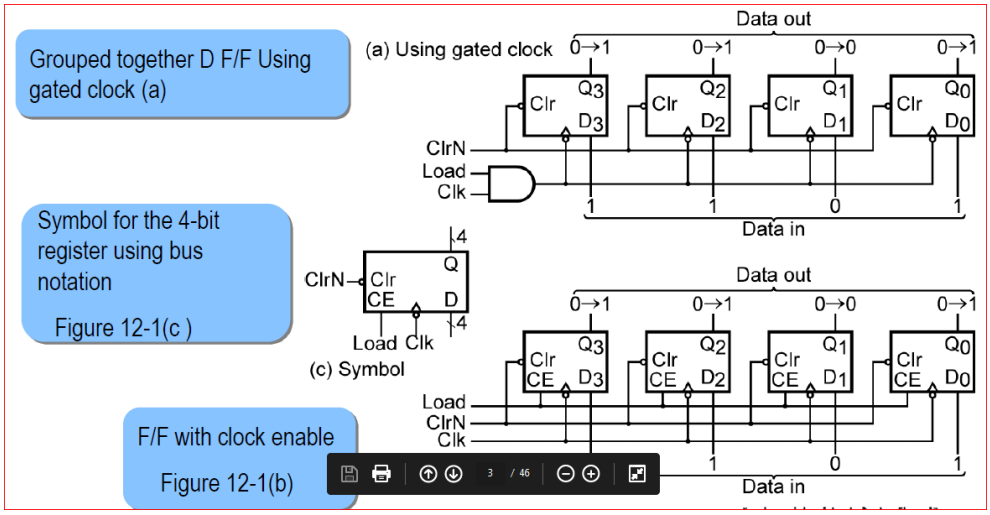
$Q^+ = JQ' + K'Q$

(b) Truth table and characteristic equation

Next state Q+ output 1 when J=1 and Q-0 or K=0 and Q=1
The J-K flip-flop (Figure above is an extended version of the S-R flip-flop.

Register

A Register is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data.



When it is time to load data into register, Load is set to 1 for one clock period. When, Load = 1, the clock signal (Clk) is transmitted to the FF clock inputs and the data applied to the D FF inputs will be loaded into the FFs on the falling edge of the clock. E.g., if the outputs are 0000 (Q3 = Q2 = Q1 =Q0 = 0) and the data inputs are 1101 (D3 = 1, D2 = 1, D1 = 0, D0 = 1), after the falling edge of the clock Q will change from 0000 to 1101. ClrN is the clear signal. A logic 0 is required to clear the FF.

Q7

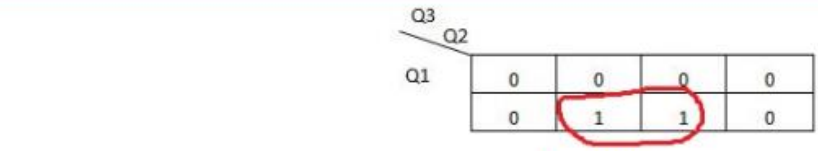
T Flip Flop Excitation Table

PRESENT STATE	NEXT STATE	T
0	0	0
0	1	1
1	0	1
1	1	0

So, the above table is the excitation table for T Flip Flop.

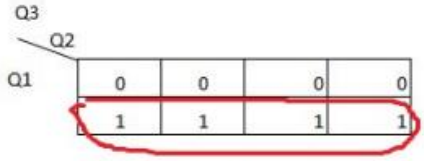
State Table with excitation table

PRESENT STATE			NEXT STATE			FLIP FLOP		
Q_3	Q_2	Q_1	Q'_3	Q'_2	Q'_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



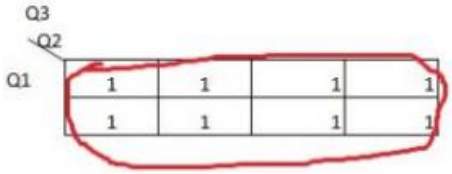
$T_3 = Q_1.Q_2$

For T_2 Flip flop,

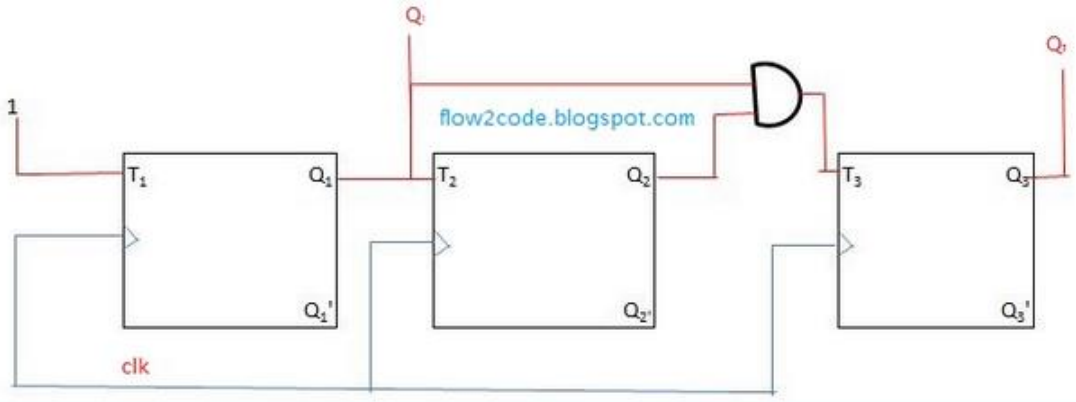


$T_2 = Q_1$

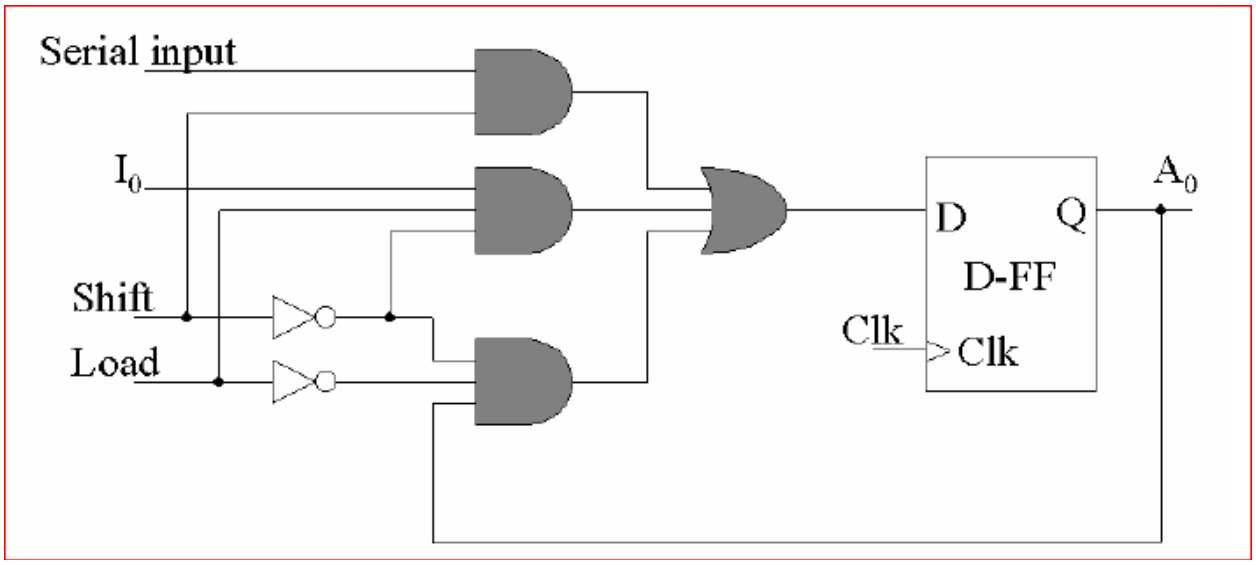
For T_1 Flip flop,



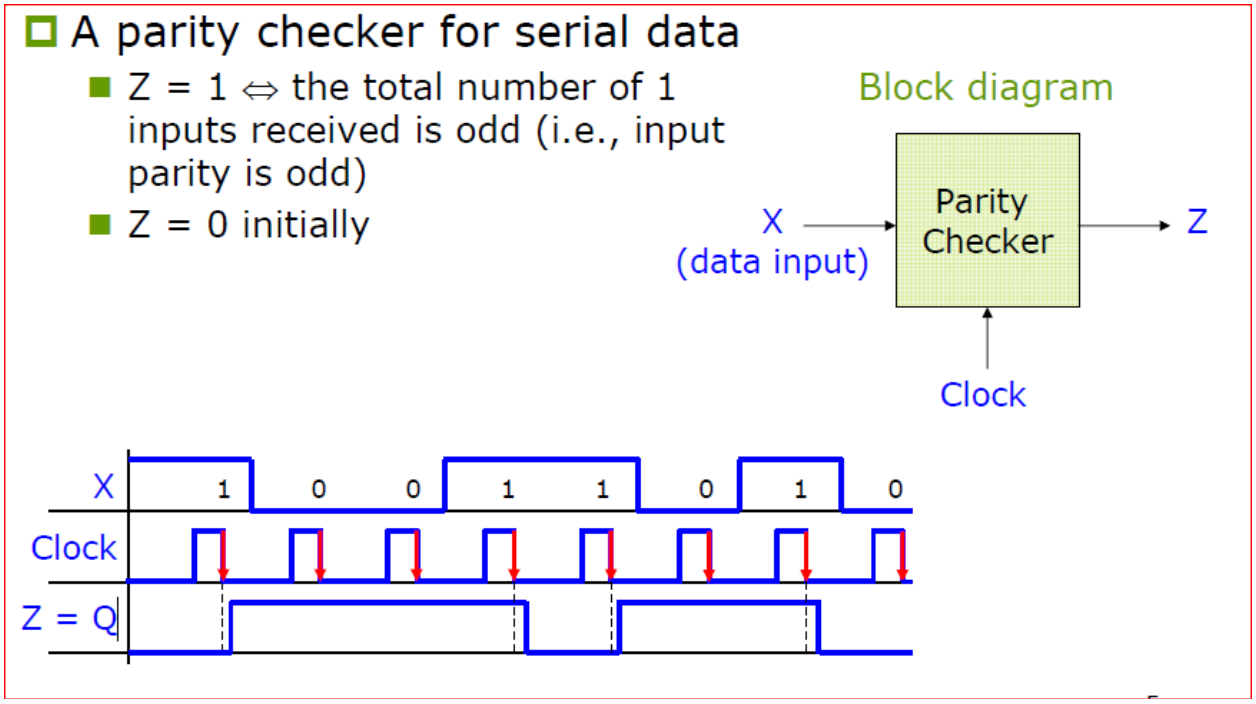
$T_1 = 1$



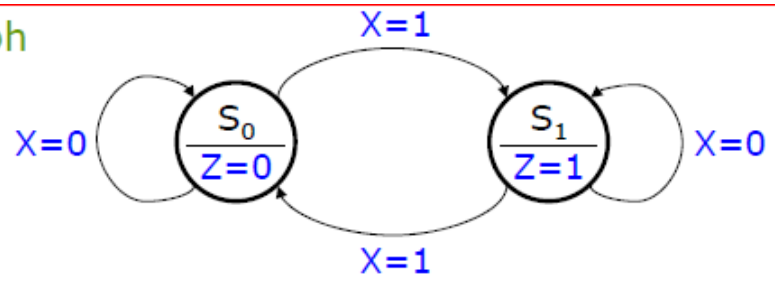
Q8 Design a 4-bit shift register with parallel load using *D flip-flops.* These are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register dose not change.


Serial input
I_0
Shift
Load
D
Q
D-FF
Clk
Clk
A_0

Q9Answer:


A parity checker for serial data
Z = 1 ⇔ the total number of 1 inputs received is odd (i.e., input parity is odd)
Z = 0 initially
Block diagram
X
(data input)
Parity Checker
Z
Clock
X
Clock
Z = Q
1 0 0 1 1 0 1 0

State graph

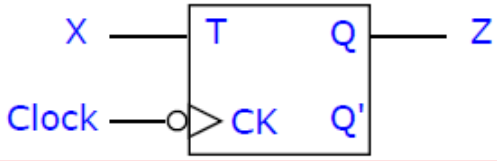


State table

Present State	Next State X=0	Next State X=1	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

Q	Q^+ X=0	Q^+ X=1	T X=0	T X=1	Z
0	0	1	0	1	0
1	1	0	0	1	1

Logic circuit



Q10 ParallelAdder

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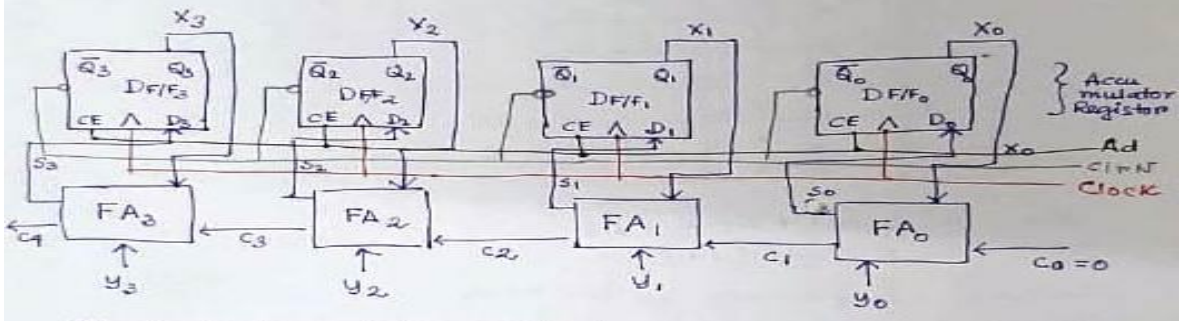
A single full adder performs the addition of two one bit numbers and an input carry. But a Parallel Adder is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. It consists of full adders connected in a chain **where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain.** A n bit parallel adder requires n full adders to perform the operation. **So for the two-bit number, two adders are needed while for four bit number, four adders are needed and so on. Parallel adders normally incorporate carry lookahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed.**

Answer: An accumulator is a register for storing short-term & intermediate data generated from any arithmetic or logical data processing or operation.



The circuit shows 4-bit parallel binary adder using a register of flip flops are known as accumulator. In this design A full adder circuit is used for parallel addition. Initially, carry (C_0) is assumed to be zero, i.e., $C_0 = 0$ which is applied to the first Full adder i.e., FA0. The 'Ad' signal is used to load the adder o/p into the accumulator on the rising edge of clock. Initially, 4-bit number $X_3\ X_2\ X_1\ X_0$ (augend) is stored in the accumulator. The number ($Y_3\ Y_2\ Y_1\ Y_0$) (addend) is applied to the accumulator after carry propagation to the adder.

hence,

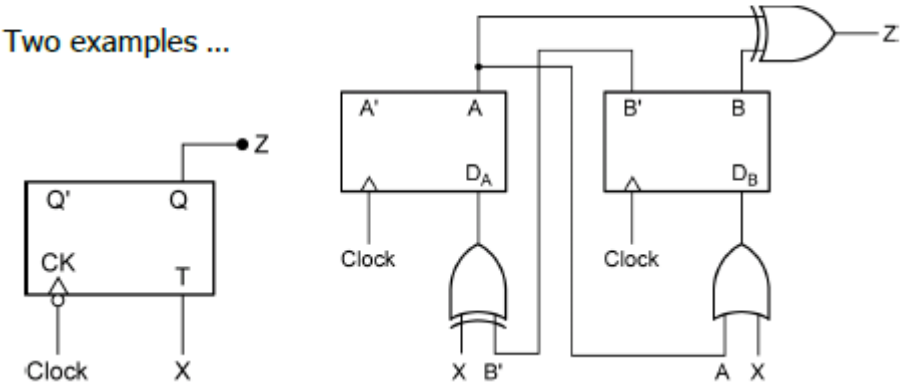
Accumulator	=	X_3	X_2	X_1	X_0 (augend) at time t_0
addend	+	Y_3	Y_2	Y_1	Y_0 at time t_0
Sum	=	S_3	S_2	S_1	S_0

If $S_i = 1$, after applying this signal into D F/F at active edge of clock signal $Q^+ = 1$, else, $S_i = 0$ then $Q^+ = 0$.

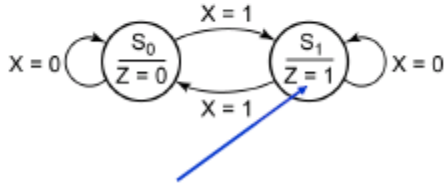
This sum $S_3\ S_2\ S_1\ S_0$ is stored in respective F/Fs and in the next iteration at the same value will be used as an augend.

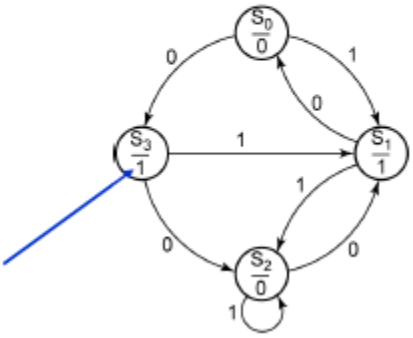
time to	augend	=	X_3	X_2	X_1 X_0
	addend	=	Y_3	Y_2	Y_1 Y_0
	accumulator	=	S_3	S_2	S_1 S_0
at time t_1	augend	=	S_3	S_2	S_1 S_0
	addend	=	Y_3'	Y_2'	Y_1' Y_0'
	accum.	=	S_3'	S_2'	S_1' S_0'
at time t_2	augend	=	S_3'	S_2'	S_1' S_0'
	addend	=	Y_3''	Y_2''	Y_1'' Y_0''
	acc.	=	S_3''	S_2''	S_1'' S_0'' and so on.

- Moore machine ...
  - Output of a sequential circuit is a function of the present state only
  - Two examples ...



  - The state graph for a Moore machine has the output associated with the state





- Analyze the circuit below ... input sequence X = **0**1101 ... Initial state is A = B = 0
- Initially ... X = 0 ... so $D_A = 1$ ... and ... $D_B = 0$
- The state will change to A = 1 and B = 0 after the first rising clock edge