CBCS SCHEME

USN | | | | | | | | | |

21CS33

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive an expression for collector current and collector emitter voltage of voltage divider bias circuit (accurate analysis). **(08 Marks)**

b. Explain relaxation oscillator. **(06 Marks)**

c. Sketch and explain the working of Peak detector. **(06 Marks)**

OR

2 a. Explain R-2R ladder type DAC with a neat diagram. **(06 Marks)**

b. List the advantages of active filters over passive filters. **(06 Marks)**

c. For the circuit shown in Fig. Q2 (c) below find the value of R_1 and R_2 if supply voltages are +12 and −12 V. Assume hysteresis with −6 V.

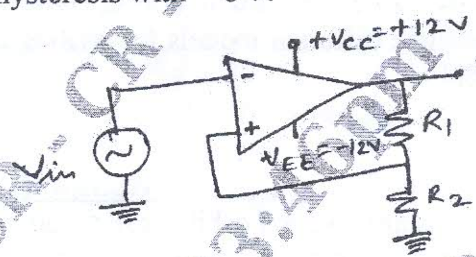

Fig. Q2 (c) **(08 Marks)**

Module-2

3 a. Find all the prime implicates of the function,
$f(a,b,c,d) = \Pi(0,2,3,4,5,12,13) + \Pi d(8,10)$
using the Quine-McCluskey method. **(10 Marks)**

b. Plot the Karnaugh maps and find all the minimal sums and minimal products of the following Boolean functions.

(i) $f(a,b,c) = \sum(2,4,5,6,7)$

(i) $f(a,b,c) = \Pi(1,4,5,6)$ **(10 Marks)**

OR

4 a. With an example, explain Petrik's method. **(06 Marks)**

b. For the given Boolean function, determine a minimal sum and a minimal product using MEV techniques using a, b and c as the map variables.
$f = \sum(3,4,5,7,8,11,12,13,15)$ **(08 Marks)**

c. Explain Entered variable map method. **(06 Marks)**

Module-3

5 a. Explain the importance of three-state buffer. (06 Marks)
b. With a neat diagram, explain 3 to 8 line decoder. (06 Marks)
c. What is a multiplexer? Write the logic diagram for 8 : 1 multiplexer using 4 input AND and OR gates. (08 Marks)

OR

6 a. Discuss different types of hazards in combinational circuits. (08 Marks)
b. Distinguish between combinational and sequential circuit. (06 Marks)
c. Write a note on PLA and PAL. (06 Marks)

Module-4

7 a. Explain the working of JK master slave flip-flop with a sketch, truth table and symbol. (06 Marks)
b. What is D flip flop? Illustrate the operation of the clear and preset inputs in D-flip-flop with timing diagram. (08 Marks)
c. What is VHDL? Show how to model the 4 to 1 multiplexer using a VHDL conditional assignment statement. (06 Marks)

OR

8 a. What is T-flip-flop? Show how to convert D-flip flop into T-flip-flop. (08 Marks)
b. What are the three different models for writing a module body in VHDL? Give example for any one model. (06 Marks)
c. Explain with a neat diagram, VHDL program structure. (06 Marks)

Module-5

9 a. With a neat diagram, explain 4-bit parallel adder with accumulator. (10 Marks)
b. Define counter. Design mod-5 counter using J-K flip flop. (10 Marks)

OR

10 a. With neat diagram, explain 4 bit SISO register. (08 Marks)
b. Mention the Application of shift registers. (05 Marks)
c. Explain the working of a 3 bit shift register. (07 Marks)

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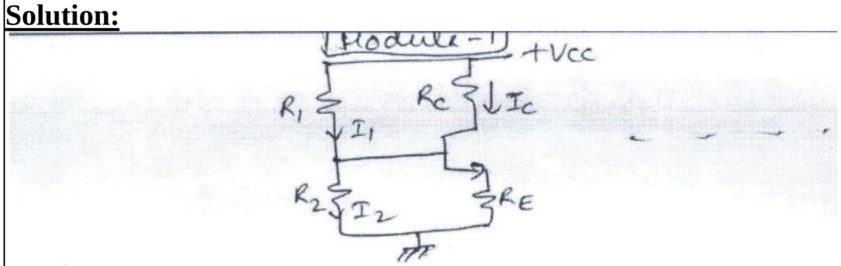
USN										

VTU Solution– March 2023

Sub:	Analog and Digital Electronics				Sub Code:	21CS33	Branch:	ISE		
Date:		Duration:	3 Hrs	Max Marks: 100	Sem/Sec:	III / A, B and C			OBE	
	Answer any FIVE FULL Questions							MARKS	CO	RBT

1 a. Derive an expression for collector current and emitter current of a voltage divider bias circuit. — 8 | CO1 | L2

Solution:



$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \quad , \quad R_T = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_T = I_B R_T + V_{BE} + I_E R_E$$
$$= I_B R_T + V_{BE} + (1+\beta) I_B R_E$$

$$\therefore I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta) R_E}$$

KVL in collector path,

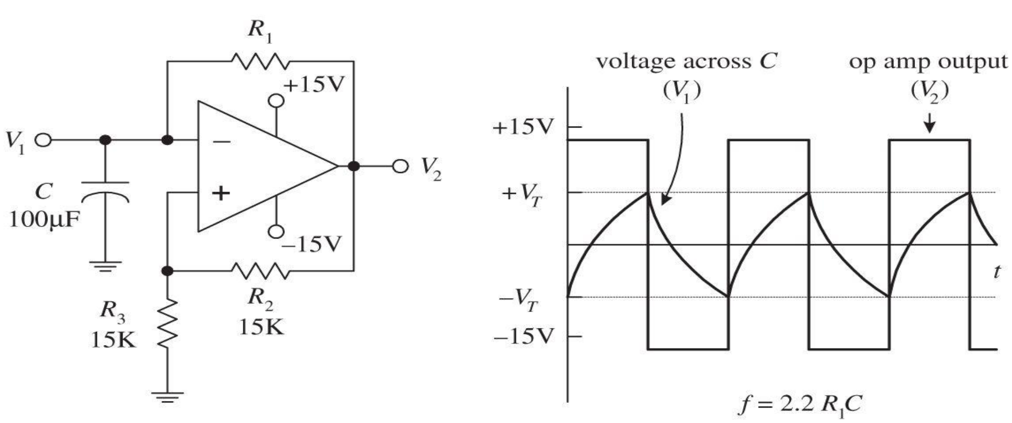
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

b. Explain relaxation oscillator — 6 | CO1 | L3

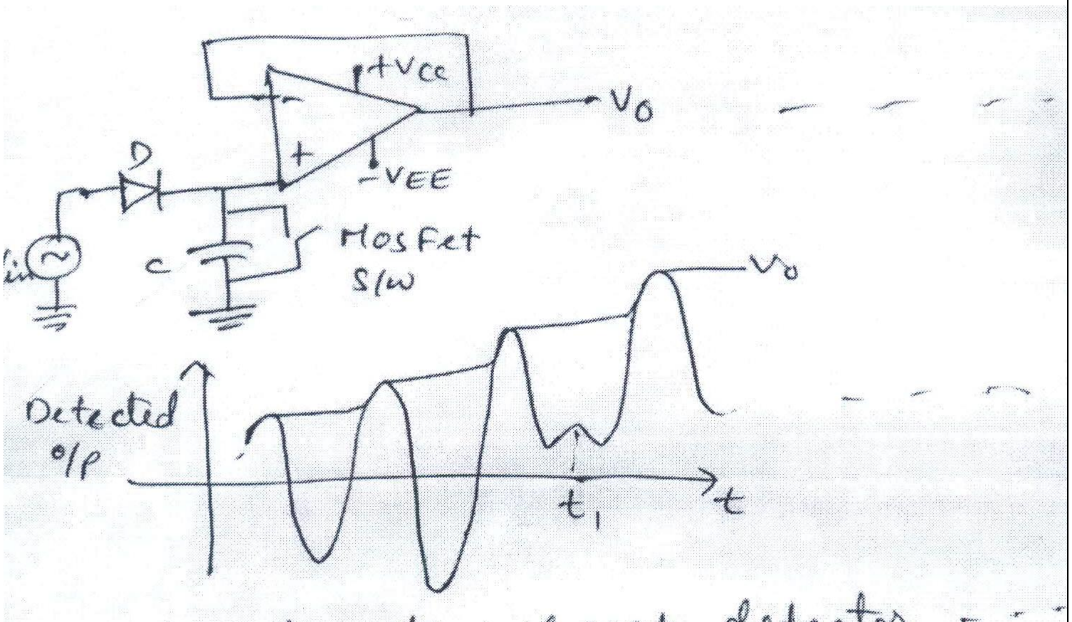
Solution:

Simple Square-Wave Relaxation Oscillator



Oscillator generally refers to the circuit which produces periodic and repetitive output like a sine wave or square wave. An oscillator can be a mechanical or electronic construction that produces oscillation depending on a few variables.

	c. Sketch and explain the working of peak detector	6		

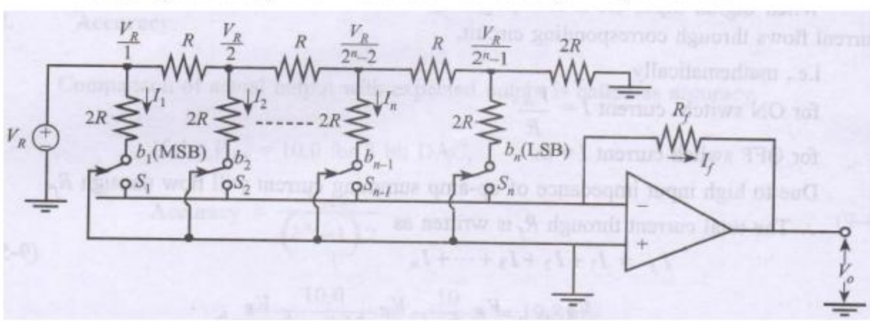


explanation of peak detector - - -

2	a. Explain R2R ladder type of ADC with a neat diagram	08	CO1	L2

Solution:

In R-2R ladder, only two values, R and 2R are used. The circuit diagram is given below:



Each binary bit connects switch either to ground (non-inverting input) or to the inverting terminal of Op-Amp. Due to virtual ground, both the positions of the switches are at ground potential, and currents through the resistances are constant.

The current flowing through each of 2R resistances;

$$I_1 = \frac{V_R}{2R} \qquad I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} \qquad I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} \qquad I_n = \frac{V_R/(2^n-1)}{2R}$$

$$\text{But, } V_0 = -I_f R_f = -R_f(I_1 + I_2 + \dots + I_N)$$

$$i.e., V_0 = -R_f\left[\frac{V_R}{2R}b_1 + \frac{V_R}{4R}b_2 + \dots + \frac{V_R}{2^n R}b_n\right]$$

$$\text{Or, } V_0 = -\frac{V_R}{R}R_f[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}]$$

$$\text{If } R_f = R; \qquad \boldsymbol{V_0 = -V_R[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}]}$$

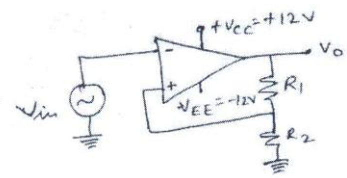
	b. List the advantage of active filter over passive filter	6	CO1	L2

Solution:

Advantage of active filters -

1. gain & freq. adjustment flexibility
2. No Loading problem
3. Cost
4. Size & weight
5. No insertion loss

	c. For the circuit shown in fig find the value of R1 and R2 if supply voltages are 12 and -12V	06		



Solution:

$$V_H = \frac{R_2 V_{sat}^{+}}{R_1+R_2} - \frac{R_1 V_{sat}^{-}}{R_1+R_2}$$

$$V_H = \frac{R_2}{R_1+R_2}\left[V_{sat}^{+} - V_{sat}^{-}\right]$$

$$\frac{V_H}{V_{sat}^{+} - V_{sat}^{-}} = \frac{R_2}{R_1+R_2} \Rightarrow \frac{6}{12-(-12)} = 0.25$$

$$\Rightarrow R_2 = 0.25R_1 + 0.25R_2$$

$$\therefore 0.75R_2 = 0.25R_1$$

$$\frac{R_2}{R_1} = \frac{0.25}{0.75}$$

Assume $R_2 = 10k\Omega$, $R_1 = 30k\Omega$

3	a. Find all the prime implicants for the function F(a,b,c,d)= Π(0,2,3,4,512,13) + Πd(8,10).	10	CO3	L2

Solution:

$$f(a,b,c,d) = \Pi(0,2,3,4,5,8,10,12,13)$$

$$\bar{f}(a,b,c,d) = \overline{M_0 \cdot M_2 \cdot M_3 \cdot M_4 \cdot M_5 \cdot M_8 \cdot M_{10} \cdot M_{12} \cdot M_{13}}$$

$$= \bar{M}_0 + \bar{M}_5 + \bar{M}_6 + \bar{M}_7 + \bar{M}_8 + \bar{M}_9 + \bar{M}_{13} + \bar{M}$$

$$= m_0 + m_2 + m_3 + m_4 + m_5 + m_8 + m_{10} + m_{12} +$$

$$f(a,b,c,d) = \Sigma(0,2,3,4,5,8,10,12,13)$$

0	$\bar{a}\bar{b}\bar{c}\bar{d}$	0000	0
2	$\bar{a}\bar{b}c\bar{d}$	0010	1
3	$\bar{a}\bar{b}cd$	0011	2
4	$\bar{a}b\bar{c}\bar{d}$	0100	1
5	$\bar{a}b\bar{c}d$	0101	1
8	$a\bar{b}\bar{c}\bar{d}$	1000	2
10	$a\bar{b}c\bar{d}$	1010	2
12	$ab\bar{c}\bar{d}$	1100	3
12	$ab\bar{c}d$	1101	3

0	0	0	0	0	✓	index 0
2	0	0	1	0	✓✓	index 1
4	0	1	0	0	✓✓	
8	1	0	0	0	✓✓	
3	0	0	1	1	✓	index 2
5	0	1	0	1	✓✓	
10	1	0	1	0	✓	
12	1	1	0	0	✓✓	
13	1	1	0	1	✓✓	index 3

0,2	0	0	–	0	✓
0,4	0	–	0	0	✓
0,8	–	0	0	0	✓
2,3	0	0	1	–	
2,10	–	0	1	0	✓
4,5	0	1	0	–	✓
4,12	–	1	0	0	✓
8,10	1	0	–	0	✓
8,12	1	–	0	0	✓
5,13	–	1	0	1	✓
12,13	1	1	0	–	✓

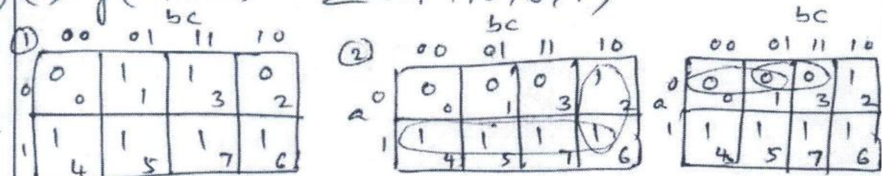
(0,2) (8,10)	–	0	–	0
(0,4) (8,12)	–	–	0	0
(4,5) (12,13)	–	1	0	–

$\bar{a}\bar{b}c$	$\bar{a}+b+\bar{c}$
$\bar{b}\bar{d}$	$b+d$
$\bar{c}\bar{d}$	$c+d$
$b\bar{c}$	$\bar{b}+c$

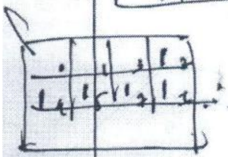
	Question	Marks	CO	Level
	Plot the Karnaugh maps and find all the minimal sums and minimal products of the following Boolean functions. (i) $f(a,b,c) = \sum(2,4,5,6,7)$ (i) $f(a,b,c) = \Pi(1,4,5,6)$ **(10 Marks)**	10	CO3	L2

Solution:

b) (a) $f(a,b,c) = \Sigma(2,4,5,6,7)$



1-map 0-map



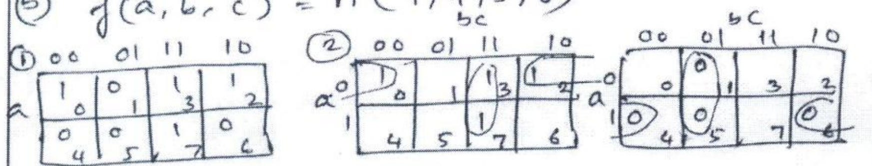
$\therefore$ minimal sum is

$f(a,b,c) = a + b\bar{c}$

minimal product is

$f(a,b,c) = (a+b)(a+\bar{c})$

(b) $f(a,b,c) = \pi(1,4,5,6)$



minimal sum is

$f(a,b,c) = \bar{a}\bar{c} + bc$

minimal product

$f(a,b,c) = (\bar{a}+c)(b+\bar{c})$

	Question	Marks	CO	Level
4	**a.** Explain petricks method	6	CO3	L2

Solution:

Petrik's method.

		m_2 $\bar{a}b\bar{c}$	m_3 $\bar{a}bc$	m_4 $a\bar{b}\bar{c}$	m_5 $a\bar{b}c$	m_7 abc
w	$\bar{a}b$	×	×			
x	$a\bar{b}$			×	×	
y	ac				×	×
z	bc					×

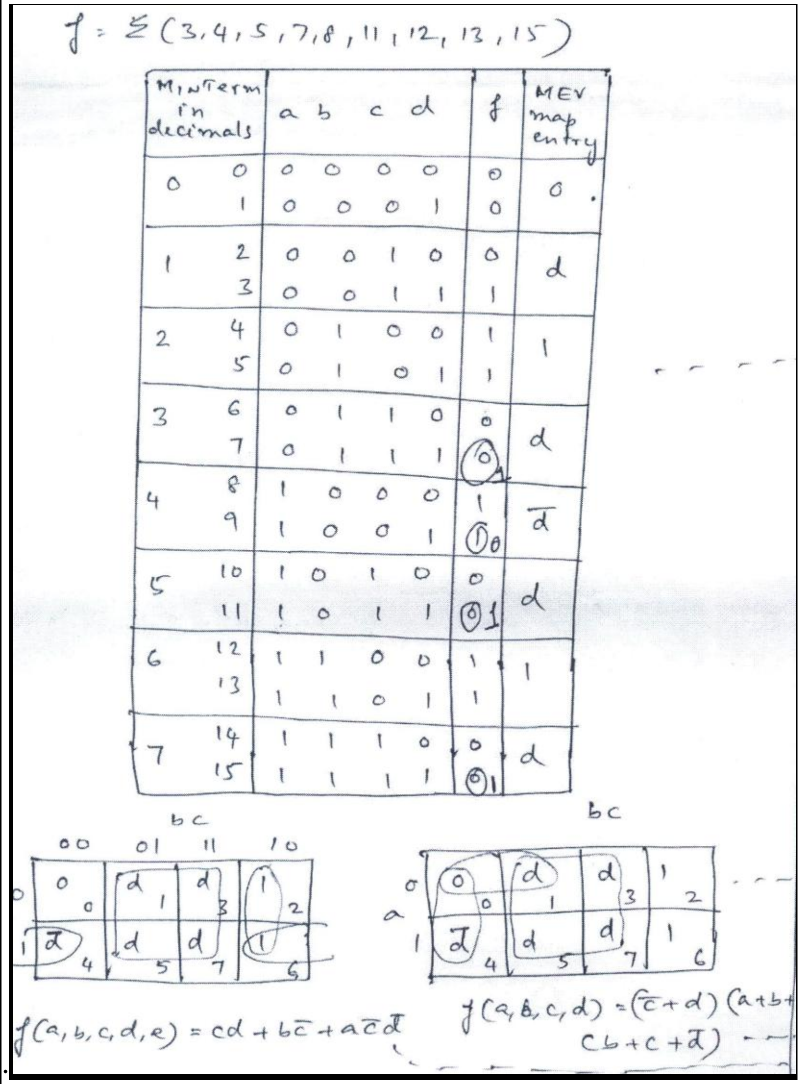
$p = m_2 \cdot m_3 \cdot m_4 \cdot m_5 \cdot m_7$

$p = (w)(w)(x)(x+y)(y+z)$

$= (w)(x+xy)(y+z)$

$p = wx(y+z) = wxz + wxz$

	b. Apply MEV method to find the essential prime implicants for the Boolean expression f(a,b,c,d)= Σm(3,4,5,7,11,12,13,15)	8	CO1	L2



$f = \Sigma(3,4,5,7,8,11,12,13,15)$

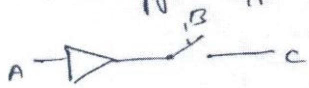
MINTERM in decimals		a	b	c	d	f	MEV map entry
0	0	0	0	0	0	0	0
	1	0	0	0	1	0	
1	2	0	0	1	0	0	d
	3	0	0	1	1	1	
2	4	0	1	0	0	1	1
	5	0	1	0	1	1	
3	6	0	1	1	0	0	d
	7	0	1	1	1	0	
4	8	1	0	0	0	1	$\bar{d}$
	9	1	0	0	1	1 0	
5	10	1	0	1	0	0	d
	11	1	0	1	1	0 1	
6	12	1	1	0	0	1	1
	13	1	1	0	1	1	
7	14	1	1	1	0	0	d
	15	1	1	1	1	0 1	

$f(a,b,c,d,e) = cd + b\bar{c} + a\bar{c}\bar{d}$

$f(a,b,c,d) = (\bar{c}+d)(a+b+c\,b+c+\bar{d})$

	c. Explain entered variable method Rules for entering values in MEV Karnaugh map .... explanation	8		
5	a. Explain importance of three state buffer. **Solution:**	6	CO4	L2

Importance of three State buffer –

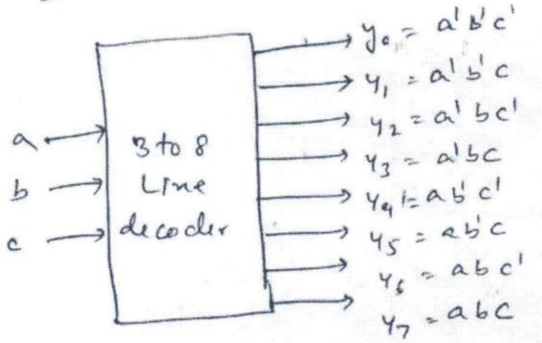
* 3 state buffers are used to select one of the sources from different sources
* If 2 nos. of 3 state buffer is connected together, if one of the buffer is disabled, the combined o/p F is the same as the other buffer o/p.
* 

when a bus is driven by 3-state buffers it is called a 3-state bus. The signals on this bus can have values 0, 1, Z & even X.

b. Explain with a neat diagram 3 to 8 line decoder. | 6 | CO4 | L1

Solution:

3 to 8 Line decoder –



a b c	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1

explanation –

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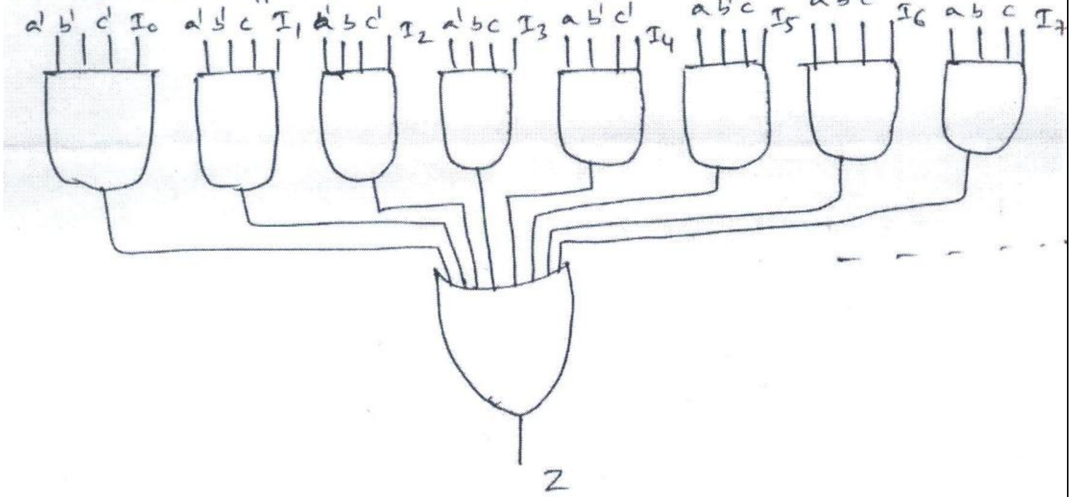
c. What is multiplxer.write the logic diagram for 8:1 multiplexer using 4 input nand gate and or gates | 8

Solution:

multiplexer has a group of data and a group of control inputs. The control inputs are used to select one of the data inputs and connect it to the o/p terminal.



$$Z = (A' + B' + C' + I_7)(A' + B' + C + I_6)(A' + B + C' + I_5)$$
$$(A' + B + C + I_4)(A + B' + C' + I_3)(A + B' + C + I_2)$$
$$(A + B + C' + I_1)(A + B + C + I_0)$$

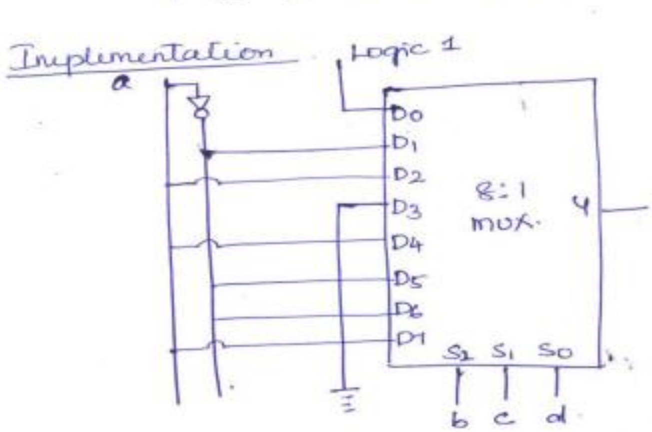
6 Write a note on hazards | 7 | CO5 | L3

Solution:

Implementation Table.

	D0	D1	D2	D3	D4	D5	D6	D7
$\bar{a}$	(0)	(1)	2	3	4	(5)	(6)	7
a	(8)	9	(10)	11	(12)	13	14	(15)
	1	$\bar{a}$	a	0	a	$\bar{a}$	$\bar{a}$	a

Implementation



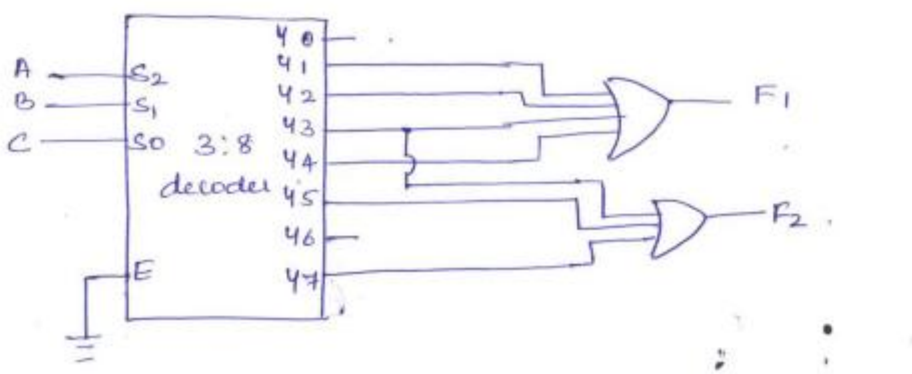
a. What is programmable logic array? How does PLA differ from PAL? | 6 | CO5 | L2

Solution:

. A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits.

S.NO	PLA	PAL
1.	PLA stands for Programmable Logic Array.	While PAL stands for Programmable Array Logic.
2.	PLA speed is lower than PAL.	While PAL's speed is higher than PLA.
3.	The complexity of PLA is high.	While PAL's complexity is less.
4.	The cost of PLA is also high.	While the cost of PAL is low.
5.	Programmable Logic Array is less available.	While Programmable Array Logic is more available than Programmable Logic Array.

		Marks	CO	Level
	c. Distinguish between sequential and combinational	7		



Q.No		Marks	CO	Level
7	a. What are the three different models for writing a module body in VHDL? Give example for any one model	6	CO2	L2

Solution:

The difference between these styles is based on the type of concurrent statements used:

- A dataflow architecture uses only concurrent signal assignment statements.
- A behavioral architecture uses only process statements.
- A structural architecture uses only component instantiation statements.

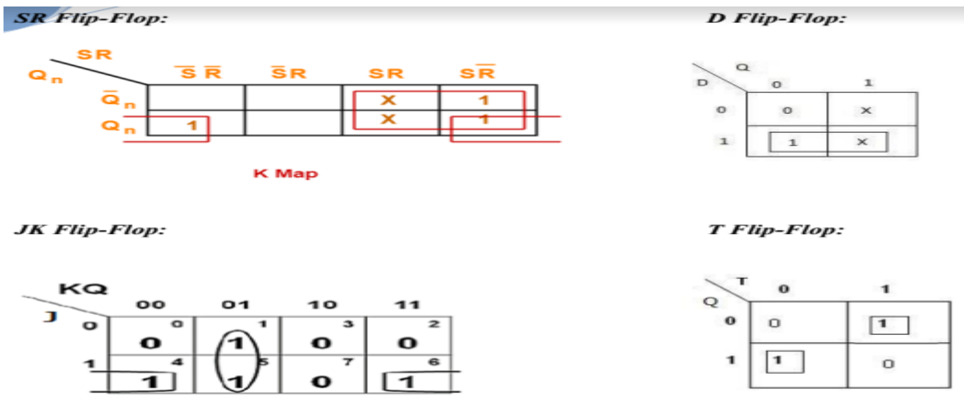
```
library ieee;
use ieee.std_logic_1164.all;

entity half_adder is
  port (a, b: in std_logic;
    sum, carry_out: out std_logic);
  end half_adder;

architecture dataflow of half_adder is
  begin
  sum <= a xor b;
  carry_out <= a and b;
end dataflow;
```

b. Derive characteristics equations for JK,T,D and SR flip flop — 8 — CO4 — L2

Solution:



The characteristic equations for the latches and flip-flops discussed so far are:

$Q^+ = S + R'Q \; (SR = 0)$ (S-R latch or flip-flop)

$Q^+ = GD + G'Q$ (gated D latch)

$Q^+ = D$ (D flip-flop)

$Q^+ = D{\cdot}CE + Q{\cdot}CE'$ (D-CE flip-flop)

$Q^+ = JQ' + K'Q$ (J-K flip-flop)

$Q^+ = T \oplus Q = TQ' + T'Q$ (T flip-flop)

c. Give VHDL code for 4:1 multiplexer using conditional assign statement. — 6

Solution:

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity mux4 is
 port(d0, d1,
 d2, d3: in STD_LOGIC_VECTOR(3 downto 0);
 s: in STD_LOGIC_VECTOR(1 downto 0);
 y: out STD_LOGIC_VECTOR(3 downto 0));
end;
architecture synth1 of mux4 is
begin
 y &lt;= d0 when s = &quot;00&quot; else
 d1 when s = &quot;01&quot; else
 d2 when s = &quot;10&quot; else
 d3;
end;
```

8 a. With a neat diagram explain VHDL Program | 6 | CO5 | L2

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Solution:

```
library ieee;
use ieee.std_logic_1164.all;

entity half_adder is                    -- Entity declaratio
  port (a, b: in std_logic;
    sum, carry_out: out std_logic);
end half_adder;

architecture structure of half_adder is     -- Architecture b

  component xor_gate                      -- xor component decl
    port (i1, i2: in std_logic;
      o1: out std_logic);
  end component;

  component and_gate                      -- and component decl
    port (i1, i2: in std_logic;
      o1: out std_logic);
  end component;

begin
   u1: xor_gate port map (i1 => a, i2 => b, o1 => sum);
   u2: and_gate port map (i1 => a, i2 => b, o1 => carry_out);
-- We can also use Positional Association
--     => u1: xor_gate port map (a, b, sum);
--     => u2: and_gate port map (a, b, carry_out);
end structure;
```

b. Derive the excitation table for JK flip flop and SR flip flop. How SR flip flop is converted to T flip flop. | 8 | CO5 | L2

Solutions:

S	R	Present state Q_n	Next state Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Invalid states (last two rows)

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation table of SR flip flop

J	K	Present state Q_n	Next state Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

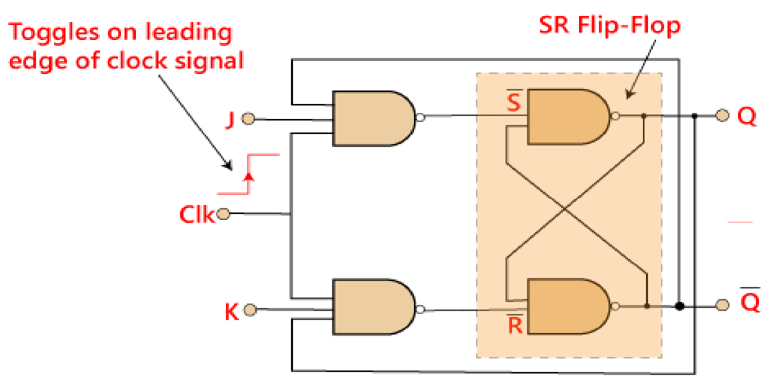
Truth table of JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table of JK flip flop

c. Explain how to convert D flip flop to T flip flop 6

Solution:



Circuit

In SR flip flop, both the inputs 'S' and 'R' are replaced by two inputs J and K. It means the J and K input equates to S and R, respectively.

The two 2-input AND gates are replaced by two 3-input NAND gates. The third input of each gate is connected to the outputs at Q and Q'. The cross-coupling of the SR flip-flop permits the previous invalid condition of (S = "1", R = "1") to be used to produce the "toggle action" as the two inputs are now interlocked.

If the circuit is "set", the J input is interrupted from the "0" position of Q' through the lower NAND gate. If the circuit is "RESET", K input is interrupted from 0 positions of Q through the upper NAND gate. Since Q and Q' are always different, we can use them to control the input. When both inputs 'J' and 'K' are set to 1, the JK toggles the flip flop as per the given truth table.

Truth Table:

	Clock	Input		Output		Description
	Clk	J	K	Q	Q'	
Same as for SR Latch	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	↓	0	1	1	0	Reset Q>>0
	X	0	1	0	1	
	↓	1	0	0	1	Set Q>>1
	X	1	0	1	0	
Toggle action	↓	1	1	0	1	Toggle
	↓	1	1	1	0	

9	a. Explain with a neat diagram parallel adder with an accumulator.	10		

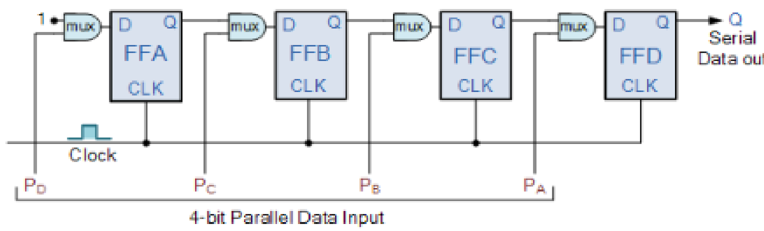
Solutions:

Parallel-in to Serial-out (PISO) Shift Register

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at P_A to P_D.

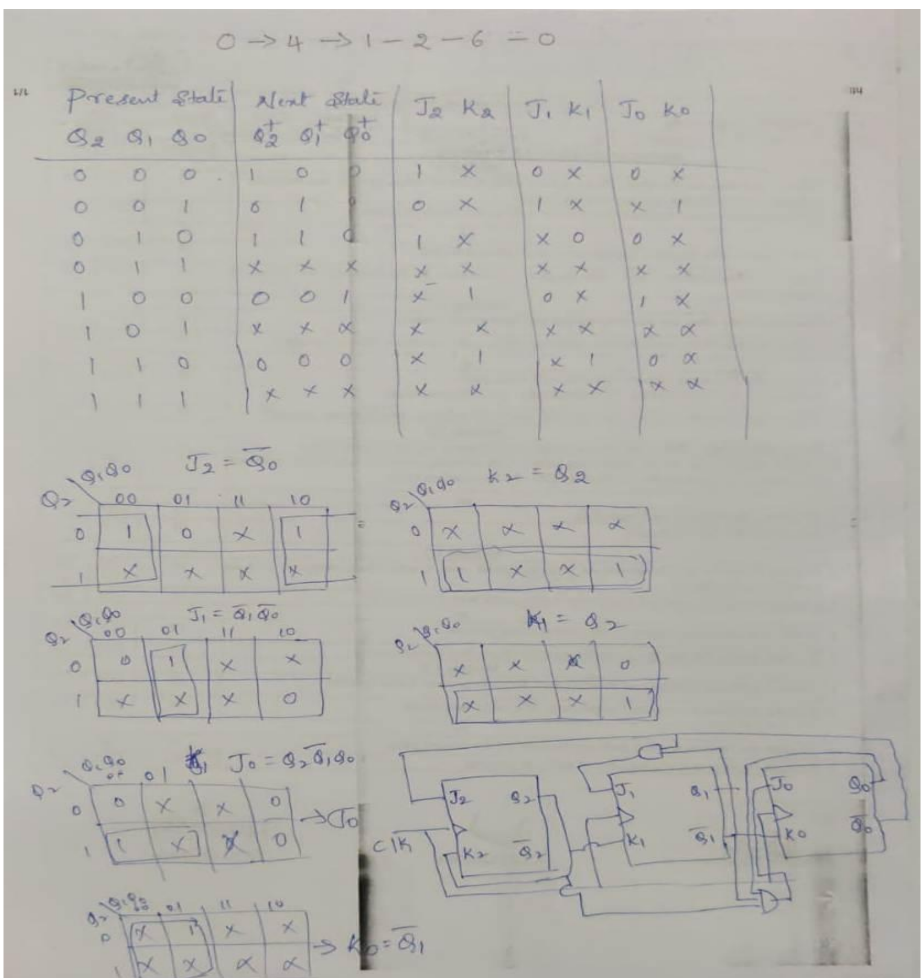
This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

4-bit Parallel-in to Serial-out Shift Register



	b. Design Mod 5 counter using JK flip flop.	10	CO4	L2

Solution:



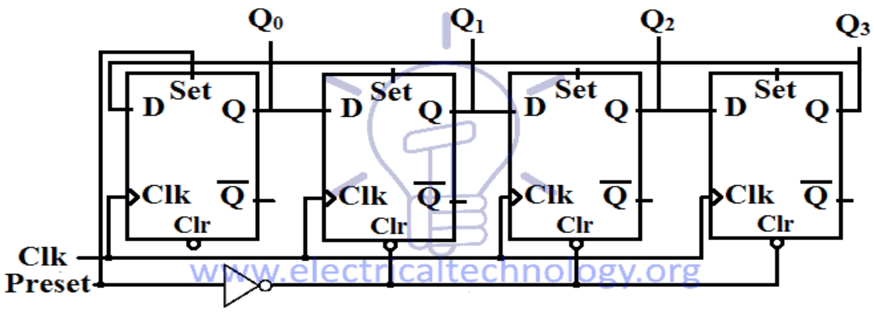
0 → 4 → 1 − 2 − 6 − 0

Q2	Q1	Q0	Q2+	Q1+	Q0+	J2	K2	J1	K1	J0	K0
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	0	1	[illegible]	0	X	1	X	X	1
0	1	0	1	1	0	1	X	X	0	0	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	0	1	X	1	0	X	1	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

$J_2 = \bar{Q}_0$ $K_2 = Q_2$

$J_1 = \bar{Q}_1 Q_0$ $K_1 = Q_2$

$J_0 = Q_2 \bar{Q}_1 \bar{Q}_0$ $K_0 = \bar{Q}_1$

10	a. With a neat diagram, explain SISO **Solutions:** Working of Ring Counter Ring counter's state needs to be set before the operation. Since ring counter circulates 1 through all stages, and there are no external inputs except the clock signal. So we need to set its state to initial state 1000 manually. We need to set the first stage flip-flop and clear the rest of the stages to obtain the state 1000.The preset input pin is designed to do this function. The schematic of ring counter is given below:  First, we need to set the initial state 1000 through preset input. Whenever the first clock edge hits the counter the outputs of each stage shifts to the next succeeding stage. And the output of the last will shift to the first stage making the state 0100. Upon next clock cycle, each stage will update its state according to its input. So the '1' will be shifted to the third stage making the state 0010. Upon another clock cycle, the '1' will reach the last stage making the 0001. Now upon next clock cycle, '1' from the last stage (flip-flop) will shift back to the first stage making the initial state 1000. And it starts again from the first state repeating itself considering the clock signal is provided. This is how the data inside the ring counter circulates in the ring. Ring counter divides the frequency of the clock signal by 'n'. n is the bit size of the ring counter. So ring counter can be used as a frequency divider.	6	CO5	L2
	b. Mention application of shift register **Solutions:** **Step 1:** Determine the number of flip flop needed Flip flop required are $2^n \geq N$ Mod 5 hence N=5 $\therefore 2^n \geq N$ $\therefore 2^n \geq 5$ $N = 3$ i.e. 3 flip flop are required **Step 2:** Type of flip flop to be used: JK flip flop **Step 3:** **1) Excitation table for JK flip flop**	8	CO1	L2

Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1

Now, we can derive excitation table for counter using above table as follows:

2) Excitation table for counter

Present state			Next state			Flip flop Input					
Q_c	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_a
0	0	0	0	0	1	×	0	0	×	1	×
0	0	1	0	1	0	×	1	1	×	×	1
0	1	0	0	1	1	×	×	×	0	1	×
0	1	1	1	0	0	×	×	×	1	×	1
1	0	0	0	0	0	1	0	0	×	0	×
1	0	1	×	×	×	×	×	×	×	×	×
1	1	0	×	×	×	×	×	×	×	×	×
1	1	1	×	×	×	×	×	×	×	×	×

Step 4

K-map simplification

For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	x	x	x	x

$J_c = Q_BQ_A$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	x	x	x	x
1	1	x	x	x

$K_C = 1$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	×	×	1	0
1	×	×	×	×

$K_B = QA$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	×	×	1
1	0	×	×	×

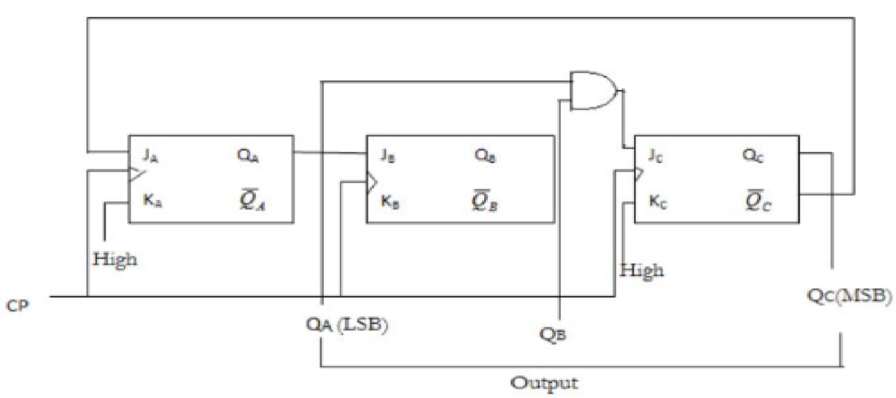
$J_A = \overline{Q}_C$

For K_A

Q_C \ Q_BQ_A	00	01	11	10
0	×	1	1	×
1	×	×	×	×

$K_A = 1$

Step 5 Logic Diagram



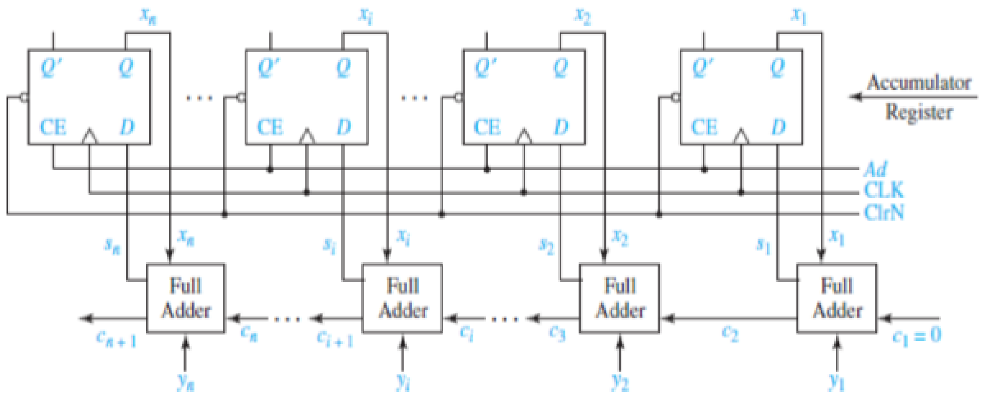
c. Explain the working of three bit shift register. 6

Solution:

Parallel Adder with Accumulator:

In computer circuits, it is frequently desirable to store one number in a register of flip-flops (called an accumulator) and add a second number to it, leaving the result stored in the accumulator.

One way to build a parallel adder with an accumulator is to add a register to the adder as shown in the following Figure.



Suppose that the number $X = x_n \dots x_2x_1$ is stored in the accumulator. Then, the number $Y = y_n \dots y_2y_1$ is applied to the full adder inputs, and after the carry has propagated through the adders, the sum of X and Y appears at the adder outputs. An add signal (Ad) is used to load the adder outputs into the accumulator flip-flops on the rising clock edge. If $s_i = 1$, the next state of flip-flop x_i will be 1. If $s_i = 0$, the next state of flip-flop x_i will be 0.Thus, $x_i^+ = s_i$, and if $Ad = 1$, the number X in the accumulator is replaced with the sum of X and Y, following the rising edge of the clock.

Observe that the adder with accumulator is an iterative structure that consists of a number of identical cells. Each cell contains a full adder and an associated accumulator flip-flop. Cell i, which has inputs c_i and y_i and outputs $c_i = 1$ and x_i, is referred to as a typical cell.

Before addition can take place, the accumulator must be loaded with X. This can be accomplished in several ways. The easiest way is to first clear the accumulator using the asynchronous clear inputs on the flip-flops, and then put the X data on the Y inputs to the adder and add to the accumulator in the normal way. Alternatively, we could add multiplexers at the accumulator inputs so that we could select either the Y input data or the adder output to load into the accumulator. This would eliminate the extra step of clearing the accumulator but would add to the hardware complexity.