CBCS SCHEME

USN | | | | | | | | | | |

21EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the classical discrete circuit bias (voltage divider bias) method of BJT. **(08 Marks)**

b. Explain the three biasing methods to bias MOS Amplifier circuits. **(12 Marks)**

OR

2 a. Explain the T equivalent circuit model of MOSFET. **(08 Marks)**

b. Derive an expression for voltage gain of MOSFET with necessary waveforms. **(06 Marks)**

c. Explain biasing a BJT using collector to base feedback resistor. **(06 Marks)**

Module-2

3 a. Explain the common source amplifier and derive the expression for voltage gain. **(10 Marks)**

b. A transistor amplifier is fed with a signal source having an open circuit voltage Vsig of 10mV and an internal resistance risig of 100KΩ. The voltage V_i at the amplifier input and the output voltage V_0 are measured both without and with load resistance R_L = 10KΩ connected to the amplifier output. The measured results are as follows :

	V_i (mv)	V_0 (mv)
Without R_L	9	90
With R_L connected	8	70

Find all the amplifier parameters. **(10 Marks)**

OR

4 a. With a neat diagram, explain the three frequency bands of MOSFET. **(06 Marks)**

b. Explain the high frequency model of MOSFET. **(06 Marks)**

c. Explain common source follower and derive the expression of voltage gain. **(08 Marks)**

Module-3

5 a. Explain the properties of negative feedback. **(10 Marks)**

b. Explain the transformer coupled class – A power amplifier and show that efficiency is 50%. **(10 Marks)**

OR

6 a. Explain the circuit operation of class – B power amplifier and also explain the transfer characteristics. **(08 Marks)**

b. Explain the Four basic feedback topologies of the amplifier. **(12 Marks)**

Module-4

7 a. Explain R and 2R resistor digital to analog (D/A) converter and also derive the expression of output voltage. **(10 Marks)**

b. Explain the first order lowpass Butterworth filter with necessary voltage gain. **(10 Marks)**

OR

8 a. Explain the operation of monostable multivibrator. **(10 Marks)**
b. Explain the two types of Bandpass filters. **(10 Marks)**

Module-5

9 a. Explain the block diagram of power electronic system. **(06 Marks)**
b. List and explain the applications of power electronics. **(06 Marks)**
c. Explain the static anode – Cathode characteristics of SCR. **(08 Marks)**

OR

10 a. Explain the turn on methods of a Thyristor. **(10 Marks)**
b. Explain the construction and working of UJT. **(10 Marks)**

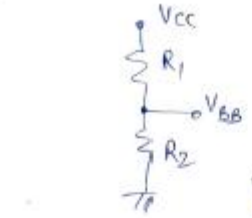
* * * * *

Module-1

1 a. Explain the classical discrete circuit bias (voltage divider bias) method of BJT. **(08 Marks)**

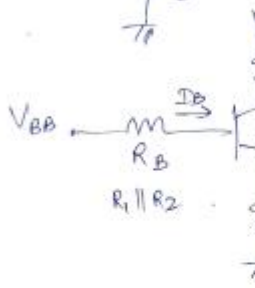
b. Explain the three biasing methods to bias MOS Amplifier circuits. **(12 Marks)**

To get Thevenin equivalent



$$V_{BB} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$



$I_C = \beta I_B$

$I_E = I_B + I_C$

$= I_B + \beta I_B$

$I_E = I_B (\beta + 1)$

$$I_B = \frac{I_E}{\beta + 1}$$

$V_{BB} = I_B R_B + V_{BE} + I_E R_E$

$$V_{BB} = \frac{I_E}{\beta+1} R_B + V_{BE} + I_C R_E$$

$$V_{BB} = I_E \left[R_E + \frac{R_B}{\beta+1} \right] + V_{BE}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$$

To make I_E insensitive to temperature variations and β variation, $R_E >> \frac{R_B}{\beta+1}$.

$V_{BB} >> V_{BE}$.

As a rule of thumb, we design for,

$$V_{BB} = \frac{1}{3} V_{CC}.$$

$$V_{CB} (\text{or } V_{CE}) = \frac{1}{3} V_{CC}. \text{ and}$$

$$I_C R_C = \frac{1}{3} V_{CC}.$$

This is required because we cannot make V_{BB} very very large. Next to get high voltage gain, the voltage V_{CB} (or V_{CE}) should be large to provide a large signal swing.

And $R_E \gg R_B$. To make I_E insensitive to variation in β could be satisfied by selecting R_B small. $\beta+1$

To make R_B small, R_1 and R_2 values should be low. Lower values of R_1 and R_2 mean a higher current drain from the power supply and will lower the input resistance of the amplifier [which is not desirable.]

The voltage divider is determining the base voltage. So the current in the voltage divider is made much larger than the base current. So we will select R_1 and R_2 in such a way that their currents is in the range of I_E to $0.1 I_E$.

4.5 Biasing in MOS Amplifier Circuits

- Establishment of an appropriate dc operating point for the transistor (MOSFET)
- To get a stable and predictable dc drain current I_D and a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

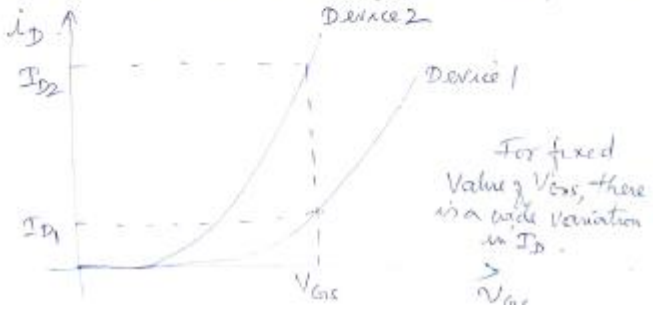
Biasing by fixing V_{GS} - If we fix V_{GS} voltage and try to provide desired I_D, it is not a good option because of the following points:-

→ We have $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$ — in saturation region

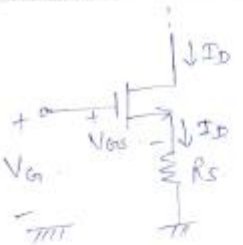
→ Values C_{ox}, V_t and $\frac{W}{L}$ vary widely among devices

→ Both V_t and μ_n depend on temperature.

→ So if we fix V_{GS}, the drain current I_D becomes very much temperature dependant as in fig below



Biasing by fixing V_G and connecting a Resistance in the Source. (18)



Fix the gate voltage V_G and connect a resistor R_S in the source as shown

$$V_G = V_{GS} + I_D R_S \quad \text{— (1)}$$

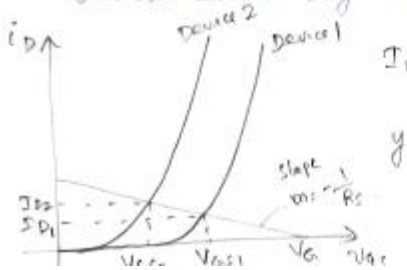
$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} - \frac{V_{GS}}{R_S}$$

If V_G is much greater than V_{GS}, then I_D will be mostly determined by the values of V_G and R_S.

$R_S \rightarrow$ provides negative feed back, which acts to stabilize the value of the bias current I_D.

If $I_D \uparrow$, V_G (constant), V_{GS} has to $\downarrow$ causing a decrease in I_D (because V_G constant)

R_S is also called degeneration resistance



$$I_D = \frac{V_G}{R_S} - \frac{V_{GS}}{R_S}$$

$y = c + mx$

$m = -\frac{1}{R_S}$

2 a. Explain the T equivalent circuit model of MOSFET. **(08 Marks)**

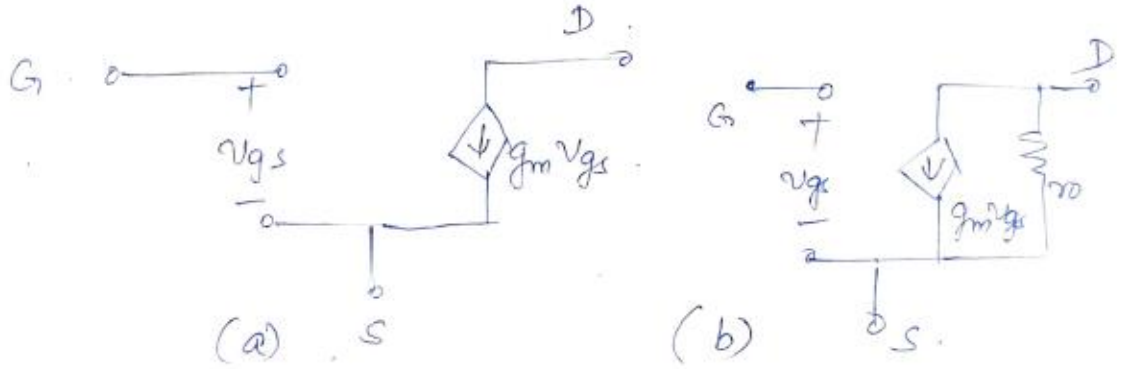
b. Derive an expression for voltage gain of MOSFET with necessary waveforms. **(06 Marks)**

c. Explain biasing a BJT using collector to base feedback resistor. **(06 Marks)**

4.6.5 Small signal equivalent circuit models

* FET behaves as a voltage controlled current source
* It accepts V_{gs} and provides $i_d = g_m V_{gs}$ at the drain terminal.
* Input resistance of MOSFET is very high, ideally infinite.
* The o/p resistance looking into the drain is also high

putting it all together, the small signal equivalent circuit is as shown below :-



Under small signal condition,

$$v_D = V_{DD} - R_D\left[i_d + I_D\right]$$

$$v_D = V_{DD} - I_D R_D - i_d R_D$$

$$v_D = V_D - i_d R_D$$

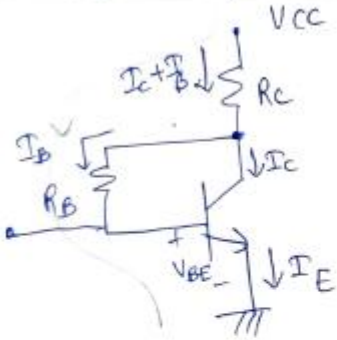
∴ The ac signal component of the drain voltage is

$$v_d = -i_d R_D$$

$$\boxed{v_d = -g_m v_{gs} R_D} \quad \text{—— (9)}$$

Voltage gain $\boxed{A_V = \frac{v_d}{v_{gs}} = -g_m R_D}$ —— (10)

Biasing using a collector to base feedback resistor (3.5.3)



R_B provides -ve feedback which helps to stabilize the bias point of BJT.

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_E R_C + \frac{I_E}{\beta+1} R_B + V_{BE}$$

$$V_{CC} = I_E\left(R_C + \frac{R_B}{\beta+1}\right) + V_{BE}$$

Also $V_{CE} = I_B R_B + V_{BE}$

$$\boxed{I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}}$$

Module-2

3 a. Explain the common source amplifier and derive the expression for voltage gain. **(10 Marks)**

b. A transistor amplifier is fed with a signal source having an open circuit voltage Vsig of 10mV and an internal resistance risig of 100KΩ. The voltage V_i at the amplifier input and the output voltage V_0 are measured both without and with load resistance R_L = 10KΩ connected to the amplifier output. The measured results are as follows :

	V_i (mv)	V_0 (mv)
Without R_L	9	90
With R_L connected	8	70

Find all the amplifier parameters. **(10 Marks)**

Solution :-

$$A_{vo} \text{ (when } R_L = \infty) = \frac{v_o}{v_i} = \frac{90}{9} = 10$$

$$G_{vo} = \frac{R_i}{R_i + R_{sig}} A_{vo} \text{ and } G_{vo} = \left.\frac{v_o}{v_{sig}}\right|_{R_L=\infty}$$

$$\therefore G_{vo} = \frac{90\,mV}{10mV} = 9. \quad \boxed{G_{vo} = 9}$$

$$9 = \frac{R_i}{R_i + 100K} \times 10. \Rightarrow \boxed{R_i = 900K\,\Omega}$$

When $R_L = 10k$ is Connected

$$A_v = \frac{70}{8} = 8.75$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{70}{10} = 7$$

To find R_o :-

$$A_v = A_{vo}\frac{R_L}{R_L + R_o}$$

$$8.75 = 10 \cdot \frac{10}{10 + R_o} \Rightarrow \boxed{R_o = 1.43k}$$

To get R_{out} :-

$$G_v = G_{vo} \cdot \frac{R_L}{R_L + R_{out}}$$

$$7 = 9 \cdot \frac{10}{10 + R_{out}} \Rightarrow \boxed{R_{out} = 2.86k}$$

To get R_{in} :-

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}}$$

$$\frac{8}{10} = \frac{R_{in}}{R_{in} + 100} \Rightarrow \boxed{R_{in} = 400k}$$

To get G_m :-

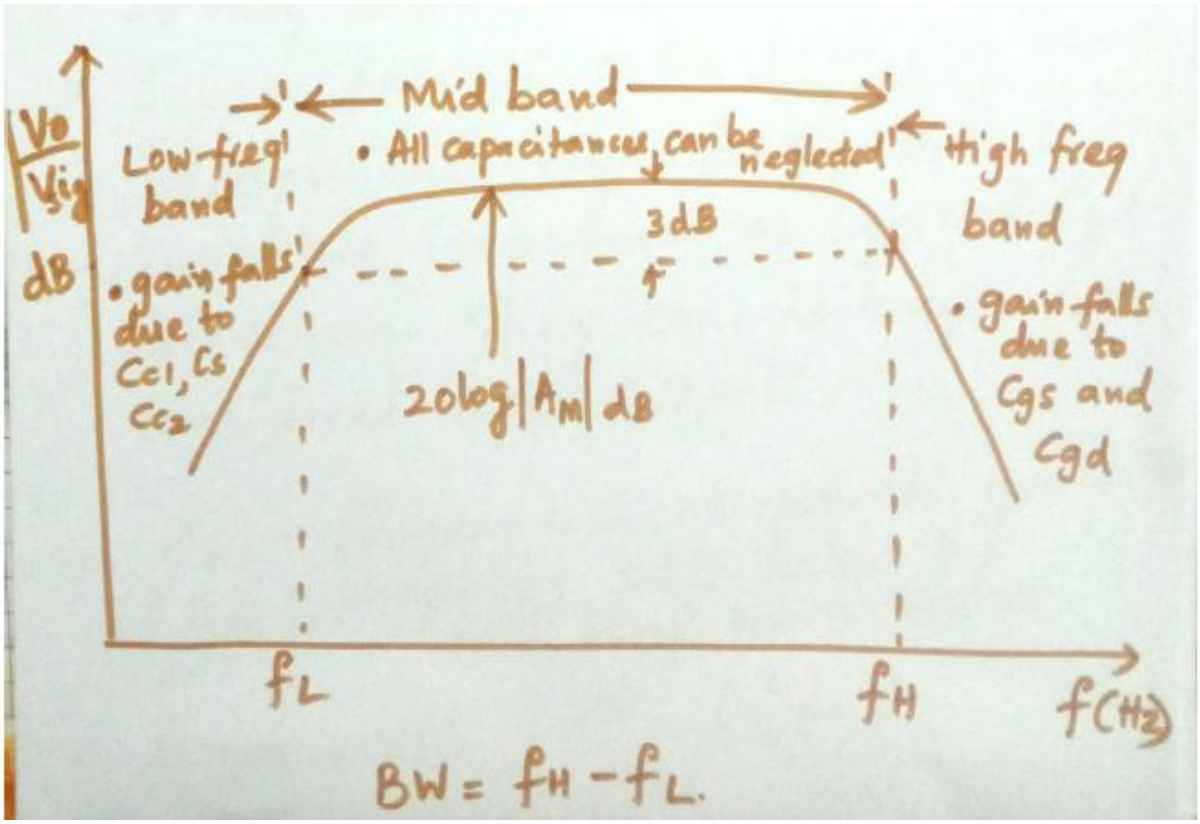
$$G_m = \frac{A_{vo}}{R_o} = \frac{10}{1.43k} = \boxed{G_m = 7mA/V}$$

OR

4 a. With a neat diagram, explain the three frequency bands of MOSFET. **(06 Marks)**

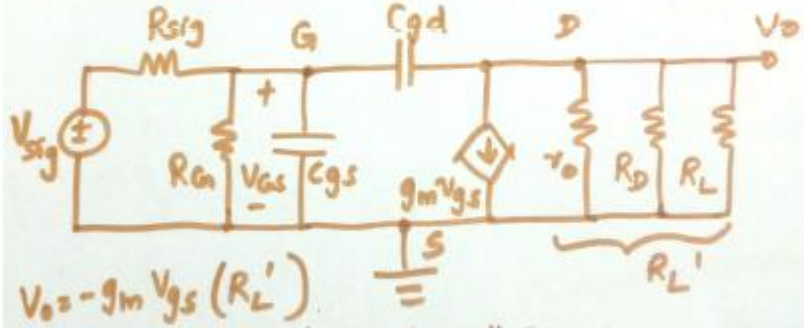
b. Explain the high frequency model of MOSFET. **(06 Marks)**

c. Explain common source follower and derive the expression of voltage gain. **(08 Marks)**



HIGH FREQ RESPONSE (4.9.2)

* At high freq, C_{c_1}, C_{c_2} C_S act as perfect short circuits
* high freq equivalent circuit of CS amplifier need to be drawn as :-



$V_o = -g_m V_{gs} (R_L')$

where $R_L' = r_o \parallel R_D \parallel R_L$.

Upper cutoff freq $f_H = \frac{1}{2\pi C_{in} R'_{sig}}$

where $C_{in} = C_{gs} + C_{gd}(1 + g_m R_L')$ * Considers both Capacitors together

$R'_{sig} = R_{sig} \parallel R_G$.

Module-3

5 a. Explain the properties of negative feedback. **(10 Marks)**

b. Explain the transformer coupled class – A power amplifier and show that efficiency is 50%. **(10 Marks)**

BW Extension

- Consider an amplifier with single pole
- A_M mid band Gain and W_H upper 3db frequency

$$A(s) = \frac{A_M}{1 + \frac{s}{w_H}}$$

- Feedback network is frequency independent

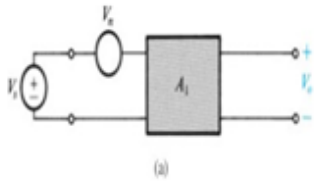
$$A_{f(s)} = \frac{A(s)}{1 + \beta A(s)}$$

$$A_{f(s)} = \frac{\frac{A_M}{1 + A_M\beta}}{1 + \frac{s}{w_H(1 + A_M\beta)}}$$

$$A_{f(s)} = \frac{A_{Mf}}{1 + \frac{s}{w_{Hf}}}$$

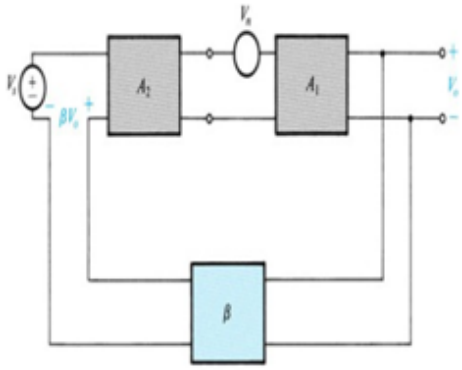
Noise Reduction

- S/N signal to Noise ratio
- Noisy stage is preceded by a noise free stage
- e.g.: Pre amplifier in case of Power amplifier stage of audio amplifier



$$\frac{S}{N} = \frac{V_s}{V_n}$$

(a)



Superposition:

$$V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta}$$

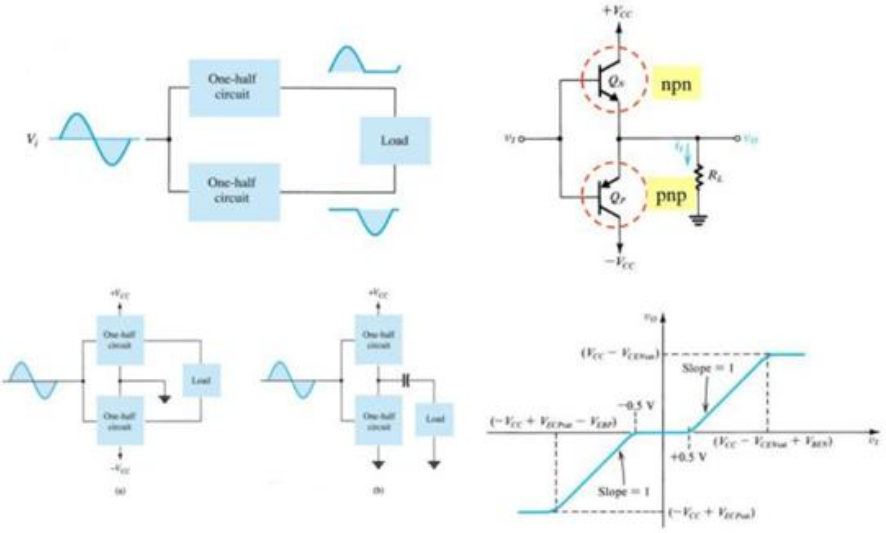
$$\left(\frac{S}{N}\right) = \frac{V_s}{V_n} A_2$$

OR

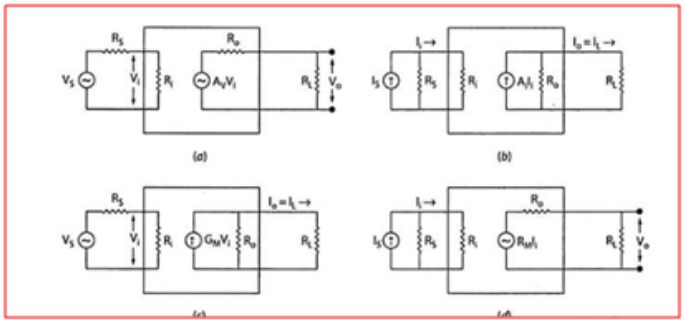
6 a. Explain the circuit operation of class – B power amplifier and also explain the transfer characteristics. **(08 Marks)**

b. Explain the Four basic feedback topologies of the amplifier. **(12 Marks)**

Class B Operation



Four basic Amplifier Configurations



Type of Amplifier	Input	Output	Transfer Gain	Ideal R_i	Ideal R_o
Voltage Amplifier	V	V	$A_V \left(= \frac{V_o}{V_i}\right)$	∞	0
Current Amplifier	I	I	$A_I \left(= \frac{I_o}{I_i}\right)$	0	∞
Transconductance Amplifier	V	I	$G_M \left(= \frac{I_o}{V_i}\right)$	∞	∞
Transresistance Amplifier	I	V	$R_M \left(= \frac{V_o}{I_i}\right)$	0	0

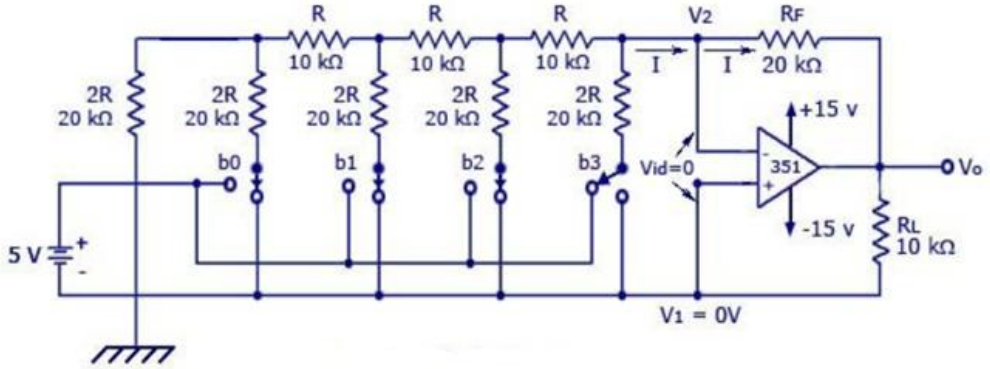
Module-4

7 a. Explain R and 2R resistor digital to analog (D/A) converter and also derive the expression of output voltage. **(10 Marks)**

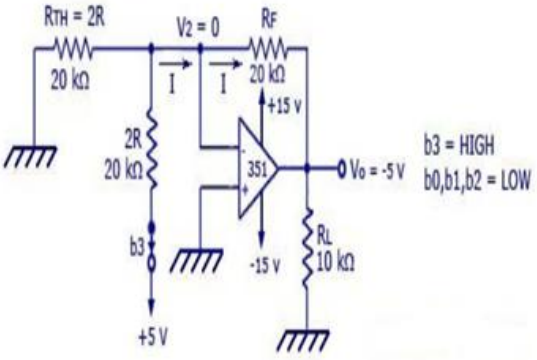
b. Explain the first order lowpass Butterworth filter with necessary voltage gain. **(10 Marks)**

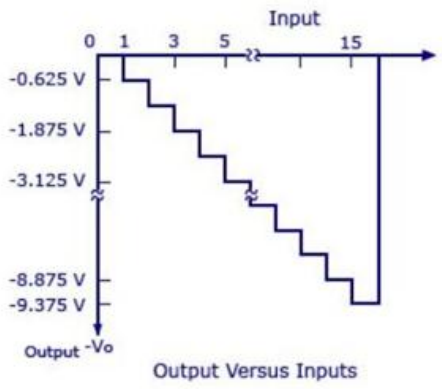
DAC:R-2R

D/A Converter With R and 2R Resistors



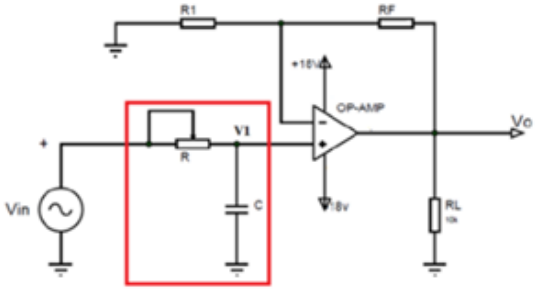
D/A Converter With R and 2R Resistors





Output Versus Inputs

First order Butterworth Low Pass Filter



$$v_1 = \frac{-jX_c}{R - jX_c} V_{in}$$

$$v_1 = \frac{V_{in}}{1 + j2\pi fRC}$$

$$v_{out} = (1 + \frac{R_f}{R_1}) \frac{V_{in}}{1 + j2\pi fRC}$$

$$\frac{v_{out}}{V_{in}} = \frac{A_F}{1 + j2\pi fRC}$$

$$\left|\frac{v_{out}}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (2\pi fRC)^2}}$$

$$A_F = (1 + \frac{R_f}{R_1})$$

$$X_C = \frac{1}{2\pi fC}$$

At Cut off freq Magnitude of gain will be $\frac{A_F}{\sqrt{2}}$

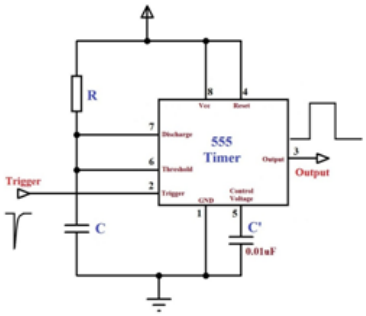
$$f_H = \frac{1}{2\pi RC}$$

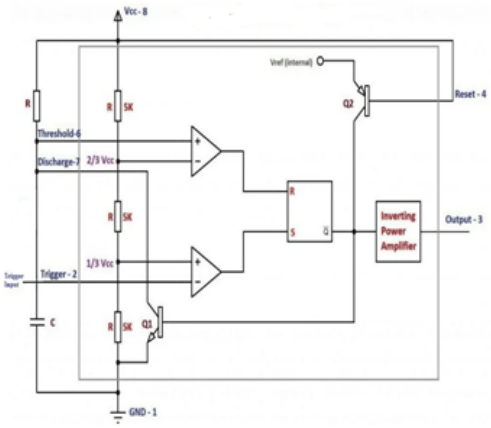
OR

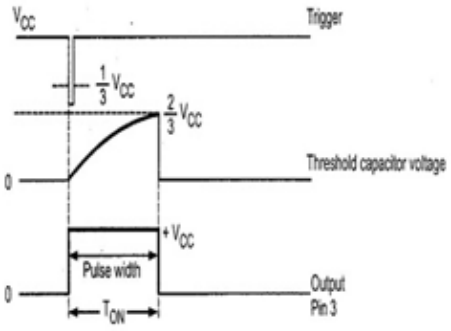
8 a. Explain the operation of monostable multivibrator. **(10 Marks)**

b. Explain the two types of Bandpass filters. **(10 Marks)**

Monostable MULTIVIBRATOR







Pulse Duration :tp/T_{ON}

$$V_C(t_p) = V_{CC} + (0 - V_{CC})e^{\frac{-t_p}{RC}}$$

$$\frac{2}{3}V_{CC} = V_{CC} - V_{CC}e^{\frac{-t_1}{RC}}$$

$$\frac{1}{3} = e^{\frac{-t_p}{RC}}$$

$$t_p = ln3 * RC$$

$$t_p = 1.1 * RC$$

Capacitor Charging equation

$$V_C(t) = V_{final} + (V_{initial} - V_{final})e^{\frac{-t}{RC}}$$

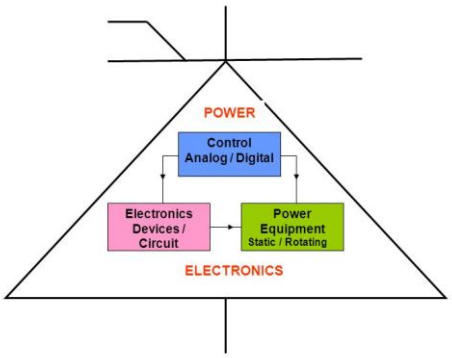
$$t_p = T_{ON} = 1.1 * RC$$

Module-5

9 a. Explain the block diagram of power electronic system. **(06 Marks)**

b. List and explain the applications of power electronics. **(06 Marks)**

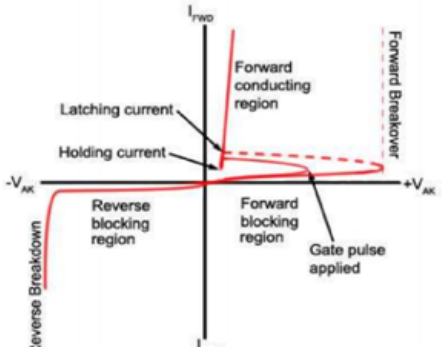
c. Explain the static anode – Cathode characteristics of SCR. **(08 Marks)**



Relationship of PE to power, electronics and control

SCR static Anode- Cathode Characteristics

- To understand the **SCR working principle** we have to look into the different ways it can operate. Depending on the polarity of the voltage applied and the gate pulse given to the SCR, it can operate in four different modes such as
- Forward Blocking mode
- Forward Conduction mode
- Reverse Blocking mode
- *Reverse Breakdown (avoided)*



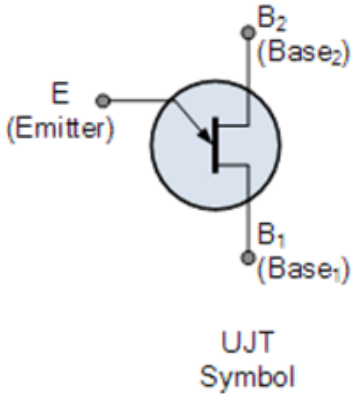
OR

10 a. Explain the turn on methods of a Thyristor. (10 Marks)
b. Explain the construction and working of UJT. (10 Marks)

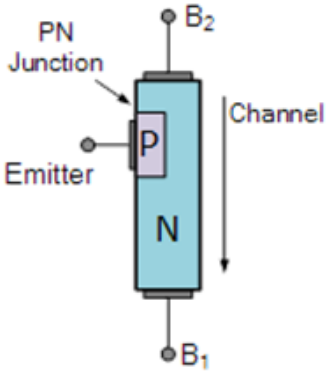
SCR Turn –ON Methods

- With a voltage applied to the SCR, if the anode is made positive with respect to the cathode, the SCR becomes forward biased. Thus, the SCR comes into the forward blocking state. The SCR can be made to conduct or switching into conduction mode is performed by any one of the following methods.
- Forward voltage triggering
- Temperature triggering (Thermal Triggering)
- dv/dt triggering
- Light triggering (Radiation Triggering)
- Gate triggering

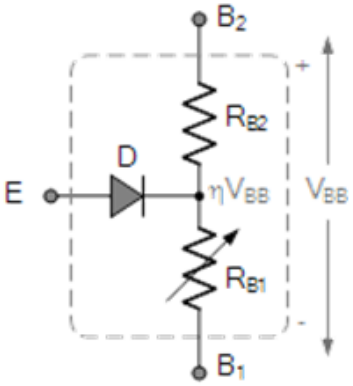
Unijunction Transistor (UJT)



UJT Symbol



Construction

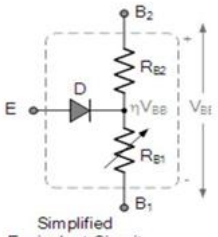


Simplified Equivalent Circuit

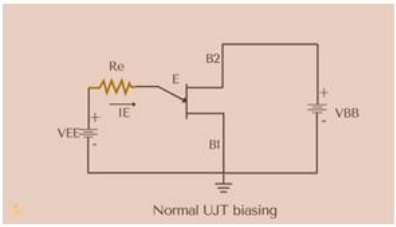
- For a Unijunction transistor, the resistive ratio of R_{B1} to R_{BB} is called the **intrinsic stand-off ratio (η)**.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

- Typical standard values of η range from 0.5 to 0.8 for most common UJT's.



Simplified Equivalent Circuit



Normal UJT biasing