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## Sixth Semester B.E. Degree Examination, June/July 2023 System Software and Compilers

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

### Module-1

- 1 a. With reference to SIC/XE machine architectures explain instruction formats and addressing modes, clearly indicating the settings of different flag bits. (10 Marks)
- b. With an illustrate example, explain the need for a two pass assembler. Explain the data structures used in 2-pass assembler. Mention their functions clearly during pass 1 and pass 2. (10 Marks)

**OR**

- 2 a. Generate the complete object program for the following SIC/XE assembly language programs. Assume : CLEAR = B4, LDT = 74, TD = EO, JEQ = 30, TIXR = B8, JLT = 38, RSUB = 4C, LDCH = 50, WD = DC, X = 1, T = 5.

```

WRREC  START      105D
        CLEAR      X
        LDT        LENGTH
WLOOP  TD         OUTPUT
        JEQ        WLOOP
        LDCH      BUFFER, X
        WD         OUTPUT
        TIXR      T
        JLT       WLOOP
        RSUB
OUTPUT  BYTE      X'05'
BUFFER  RESB      400
LENGTH  RESB      2
        END       WRREC
    
```

- b. Explain the absolute loader and Bootstrap loader with algorithm/source code. (10 Marks)

### Module-2

- 3 a. What is a Compiler? Explain the various phases of a compiler with a neat diagram and show the output of each phase for the expression  $a = b + c * 25$ . Assume all variable are a type float. (10 Marks)
- b. Write a note on the commonly used compiler – construction tools. (04 Marks)
- c. Describe Input Buffering mechanism with an algorithm for lookahead code with sentinels. (06 Marks)

**OR**

- 4 a. Construct the transition diagrams to recognize the tokens given below and explain the same.
  - i) relop    ii) Identifier    iii) unsigned numbers (10 Marks)
- b. With example, define the operations on languages. (04 Marks)
- c. Discuss the issues/errors of lexical analysis and the error recovery actions that can be performed. (06 Marks)

**Module-3**

- 5 a. What is recursive-decent parsing? Explain with a pseudocode. Take the grammar  $S \rightarrow cAd$ ,  $A \rightarrow ab|a$  as an example and trace it for input string  $w = cad$ . Explain how backtracking can be used for tracing. (10 Marks)
- b. Consider the context free grammar :  
 $S \rightarrow SS + | SS * | a$  and string  $w = aa + a*$
- Give the leftmost and rightmost derivation and parse tree for the string
  - Is the grammar ambiguous or unambiguous? Justify your answer
  - Eliminate left Recursion (10 Marks)

**OR**

- 6 a. With a neat diagram, explain the model of a table driven predictive parser. Write and explain the predictive parsing algorithm. (10 Marks)
- b. Consider the following grammar with terminals  $(, [, ), ]$ .  
 $S \rightarrow TS | [S] S | )S | \epsilon$   
 $T \rightarrow (X)$   
 $X \rightarrow TX | [X] X | \epsilon$
- Construct FIRST and FOLLOW sets
  - Construct its LL(1) parsing table
  - Is this grammar LL(1)? (10 Marks)

**Module-4**

- 7 a. Explain the meta – characters used in regular expression with examples. (10 Marks)
- b. Write a LEX program to recognize and count the number of identifiers in a given input file. Show how the program is compiled and executed. (10 Marks)

**OR**

- 8 a. What are the ambiguities that arise while evaluating a regular expression? Explain with example. (10 Marks)
- b. Write a YACC program to recognize a valid arithmetic expression that uses operators  $+$ ,  $-$ ,  $*$  and  $/$ . (10 Marks)

**Module-5**

- 9 a. What is a dependency graph? Give a syntax directed definition for simple type declaration including int and float type. Construct annotated parse tree and dependency graph for the input, float a, b, c. (10 Marks)
- b. Explain synthesized attribute, inherited attribute, S – attributed definition and L- attributed definitions with examples. (10 Marks)

**OR**

- 10 a. What is a three – address code? explain the different ways of representing three – address codes with examples. (10 Marks)
- b. What is target computer model? Explain the different kinds of instructions and addressing modes available in assembly language or a target machine. (10 Marks)

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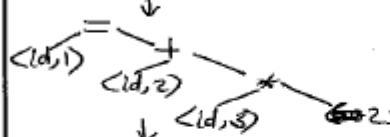
# 18CS61-System Software & Compilers

## Scheme & Solution

July 2023 Examination

1)a)	<p>Instruction formats: Format 1, 2, 3 &amp; 4</p> <p>Addressing modes: Base-relative, PC relative, direct addressing, indexed addressing, immediate addressing, indirect addressing.</p>	4M 6M																																																																						
1)b)	<p>Need for 2-pass assembler: (Explain with example)</p> <p>Pass 1 - define symbols</p> <p>Pass 2 - assemble instructions &amp; generate object program.</p> <p><u>Data Structures:</u> Location Counter, OPTAB, SYMTAB.</p>	4M 6M																																																																						
2)a)	<table border="1"> <thead> <tr> <th>Loc</th> <th>WRREC</th> <th>START</th> <th>10SD</th> <th>Object code</th> </tr> </thead> <tbody> <tr> <td>105D</td> <td></td> <td>Clear</td> <td>X</td> <td>B410</td> </tr> <tr> <td>105F</td> <td></td> <td>LDT</td> <td>Length</td> <td>77 21A7</td> </tr> <tr> <td>1062</td> <td>WLoop</td> <td>TD</td> <td>Output</td> <td>E3 2012</td> </tr> <tr> <td>1065</td> <td></td> <td>JEQ</td> <td>WLoop</td> <td>332FFA</td> </tr> <tr> <td>1068</td> <td></td> <td>LDCH</td> <td>Buffer, X</td> <td>53901078</td> </tr> <tr> <td>106C</td> <td></td> <td>WD</td> <td>Output</td> <td>DF2008</td> </tr> <tr> <td>106F</td> <td></td> <td>TIXR</td> <td>T</td> <td>B850</td> </tr> <tr> <td>1071</td> <td></td> <td>JLT</td> <td>WLoop</td> <td>382FEE</td> </tr> <tr> <td>1074</td> <td></td> <td>RESB</td> <td></td> <td>4F0000</td> </tr> <tr> <td>1077</td> <td>Output</td> <td>BYTE</td> <td>X '05'</td> <td>05</td> </tr> <tr> <td>1078</td> <td>Buffer</td> <td>RESB</td> <td>400</td> <td></td> </tr> <tr> <td>1208</td> <td>Length</td> <td>RESB</td> <td>2</td> <td></td> </tr> <tr> <td>120A</td> <td></td> <td>END</td> <td>WRREC</td> <td></td> </tr> </tbody> </table> <p>Loc - 3M Obj code - 5M Obj pgm - 2M</p> <p><u>Object Pgm:</u>  H^ WRREC^ 00105D^ 0001AD  T^ 00105D^ 1B^ B410^ 77 21A6^ E32012^  332FFA^ 53901078^ DF2008^ ^ ^ ^ 05  E^ 00105D</p>	Loc	WRREC	START	10SD	Object code	105D		Clear	X	B410	105F		LDT	Length	77 21A7	1062	WLoop	TD	Output	E3 2012	1065		JEQ	WLoop	332FFA	1068		LDCH	Buffer, X	53901078	106C		WD	Output	DF2008	106F		TIXR	T	B850	1071		JLT	WLoop	382FEE	1074		RESB		4F0000	1077	Output	BYTE	X '05'	05	1078	Buffer	RESB	400		1208	Length	RESB	2		120A		END	WRREC		
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<p>2) b)</p>	<p><u>Absolute loader</u> - does not perform linking &amp; program relocation</p> <p><u>Algorithm:</u>  begin  read: Header record  verify pgm name &amp; length  read first Text record  while record type ≠ 'E' do  begin  move obj code to specified loc in memory  read next obj pgm record  end  jump to addr specified in End record  end.</p> <p><u>Bootstrap loader</u> - loads OS &amp; begins at addr 0</p> <p>Source code of Bootstrap loader for SIC/XE</p>	<p>5M</p> <p>5M</p>
<p>3 a)</p>	<p><math>a = b + c * 25</math></p> <p>↓  <u>Lexical Analyzer</u>  &lt;id,1&gt;&lt;=&gt;&lt;id,2&gt;&lt;+&gt;&lt;id,3&gt;&lt;*&gt;&lt;25&gt;</p> <p>↓  <u>Syntax Analyzer</u></p> <p>↓  </p> <p>↓  <u>Semantic Analyzer</u>  (Same tree) * inttofloat  25</p> <p>↓  <u>Intermediate Code Gen</u>  t1 = inttofloat  t2 = id3 * t1  t3 = id2 + t2  id1 = t3</p> <p>↓  <u>Code optimizer</u>  t1 = id3 * 25.0  id1 = id2 + t1</p> <p>↓  <u>Code Generator</u></p> <p>Compiler - program that can read a pgm in one lang &amp; translate into another lang</p> <p>Explanation of phases - 5M  Example - 4M</p> <p>LDF R2, id3  MULF R2, R2, #25.0  LDF R1, id2  ADDF R1, R1, R2  STF id1, R1</p>	<p>1M</p> <p>5M</p> <p>4M</p>

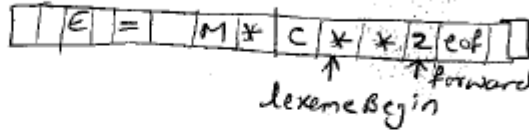
3b)

Compiler Construction tools - Parser generators, Scanner generators, Syntax-directed translation engines, Code-generator generators, Data-flow analysis engines, Compiler-construction toolkits.

4M

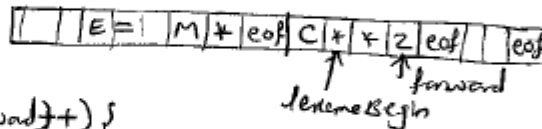
3c)

Buffer pairs:-



3M

Sentinals:



4M  
(2+2M)

```
switch (*forward++) {
```

case eof:

if (forward is at eof) {

reload 2nd buffers;

forward = beginning of 2nd buffers;

else if (forward is at eof 2nd buffer) {

reload 1st buffers;

forward = beginning of 1st buffers;

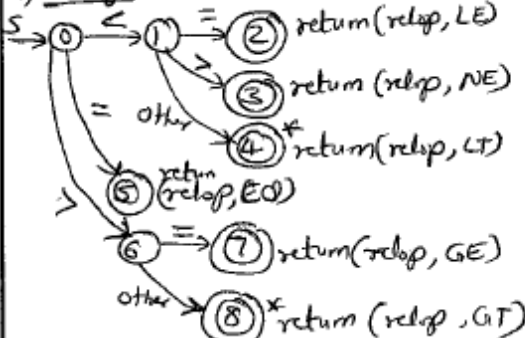
else /\* terminate \*/

break;

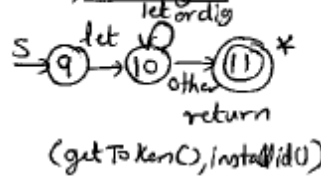
}

4a)

i) relap



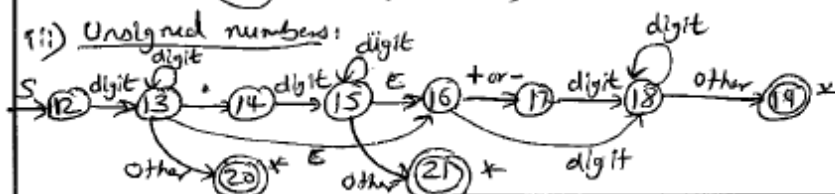
ii) identifier



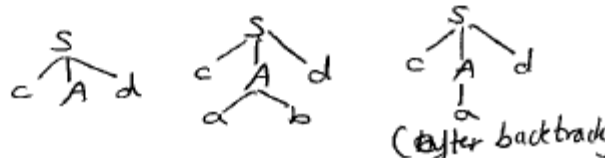
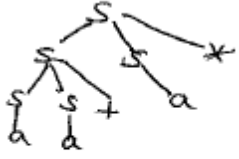
4M

2M

ii) Unsigned numbers:



4M

4b)	operations with examples: (LUM) i) Union of L & M (LUM) ii) concatenation of L & M (LM) iii) Kleene closure of L ( $L^*$ ) iv) Positive closure of L ( $L^+$ )	4M
4c)	Source-code error: $f_i(a == f(x)) \dots$ Panic-mode error. <u>Error-recovery actions:</u> i) Delete one character ii) Insert missing character iii) Replace a character iv) Transpose 2 adjacent characters.	2M  4M
5a)	<pre> void A() {   choose an A-prod, <math>A \rightarrow X_1 X_2 \dots X_k</math>;   for (i=1 to k) {     if (<math>X_i</math> is nonterminal)       call procedure <math>X_i()</math>;     else if (<math>X_i</math> equals current I/P symbol <math>a</math>)       advance I/P to next symbol;     else /* error */       ;   } } </pre> <p> <math>S \rightarrow cAd</math>  <math>A \rightarrow ab a</math> </p> 	5M  3M+2M
5b)	<p>i) <u>Leftmost</u></p> <pre> S → SS*   → SS+S*   → aS+S*   → aa+S*   → aa+a* </pre> <p><u>Rightmost</u></p> <pre> S → SS*   → Sa*   → SS+a*   → Sa+a*   → aa+a* </pre> <p>Parse tree for <math>aa+a*</math></p> 	1/2 * 4 = 6M <hr/> 1M ✓ <hr/> 3M ✓

6 a)

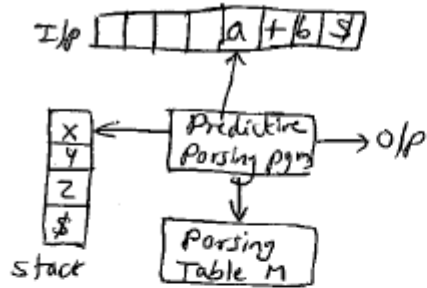


Diagram - 2M

Explanation - 3M

Algorithm: let a be 1st symbol of w;  
 let X be top of stack;  
 while (X ≠ \$) {  
   if (X = a) pop stack & let a be next symbol of w;  
   else if (X is terminal) error();  
   else if (M[X, a] is error) error();  
   else if (M[X, a] = X → Y<sub>1</sub>Y<sub>2</sub>...Y<sub>k</sub>) {  
     o/p production X → Y<sub>1</sub>Y<sub>2</sub>...Y<sub>k</sub>;  
     pop the stack;  
     push Y<sub>k</sub>, Y<sub>k-1</sub>, ..., Y<sub>1</sub> onto stack.  
   }  
 }  
 let X be top stack symbol.

Algorithm - 3M

Explanation - 2M

6 b)

1) First(S) = { (, [, ), ε }, First(T) = { ( }, First(X) = { (, ε }  
 Follow(S) = { \$, ] }, Follow(T) = { \$, [, (, ), ] }, Follow(X) = { ), ] }

2M

2M

ii) parsing table

NT	(	)	[	]	\$
S	S → TS	S → )S	S → [S]S	S → ε	S → ε
T	T → (X)				
X	X → TX	X → ε	X → [X]X	X → ε	

5M

iii) Grammar is LL(1).

1M

7 a)

Meta characters: . \* [ ] ^ \$ \ { }  
 \ + ? | " ... " / ( )

5M

Examples 5M

7 b)

```

1. { int ident = 0;
   -1;
   +1;
   [-a-zA-Z][-a-zA-Z0-9]* { printf("valid");
                           ident++; }

```

```

(^|\t|\n)+ & printf (" invalid ");
\n
}
}
}
main()
{ FILE *p;
  char fname[30];
  scanf ("%s", &fname);
  yyin = fopen (fname, "r");
  yylex();
  printf ("%d", idcnt);
}

```

Program: 8M  
Output: 2M

- 8a) Expression ambiguity with example — 3M  
 Precedence & associativity — 1M  
 Specifying implicitly — 3M  
 Specifying explicitly — 3M

```

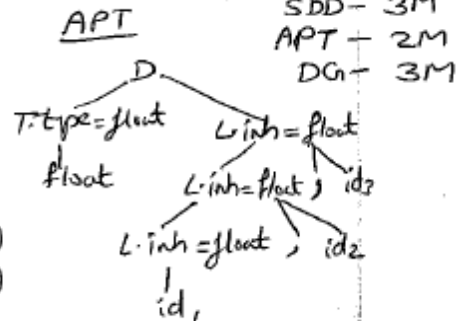
8b)
/* #include "lex.yy.c"
+3
/* tokens ID NUM
+1.
assign; ID = exp
exp : exp '+' term
    | exp '-' term
    | term
term : term '*' fac
    | term '/' fac
    | fac
fac : ID
    | NUM
+1.

/* #include "y.tab.h"
+3
+1.
[a-zA-Z]+ return ID;
[0-9]+ return NUM;
\n return 0;
return (yytok[0]);
+1.
main() yyerror()
{ ... }

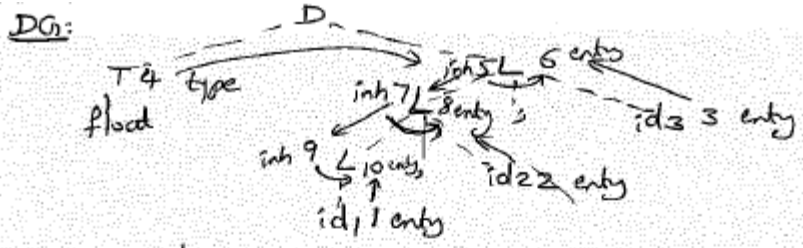
```

- 9a) Dependency graph represents interdependencies between synthesized & inherited attributes. — 2M

Production	Semantic Rules
$D \rightarrow TL$	$L.inh = T.type$
$T \rightarrow int$	$T.type = int$
$T \rightarrow float$	$T.type = float$
$L \rightarrow L_1 id$	$L_1.inh = L.inh$
	$addtype(id.entry, L.inh)$
$L \rightarrow id$	$addtype(id.entry, L.inh)$







- 9b) Synthesized attribute - defined at children & itself - 2M
- Inherited attribute - defined at parent, itself & siblings - 2M
- S-attribute Defn - every attr is synthesized - 3M
- L-attribute Defn - attribute should be synthesized or Inherited. Edges goes from left to rt. - 3M

10a) 3-address code - linearized rep<sup>n</sup> of DAG - 1M  
 $t1 = b - c$

- Representations:
- 1) Quadruples:  $op, arg1, arg2, res$  - 3M
  - 2) Triples:  $op, arg1, arg2$  - 3M
  - 3) Indirect triples: listing of pointers to triples. - 3M

10b) Target computer models a 3-address machine, with load & store operations, computation operations, jump operations & Conditional jumps & n general-purpose registers. - 1M

Instructions: Load oper<sup>n</sup>, Store oper<sup>n</sup>, unconditional jumps, computation oper<sup>n</sup>, Conditional jumps. - 4M

Addressing modes: Absolute, Indexed, Integer indexed, Indirect addressing, Immediate address. - 5M