CMR INSTITUTE OF TECHNOLOGY

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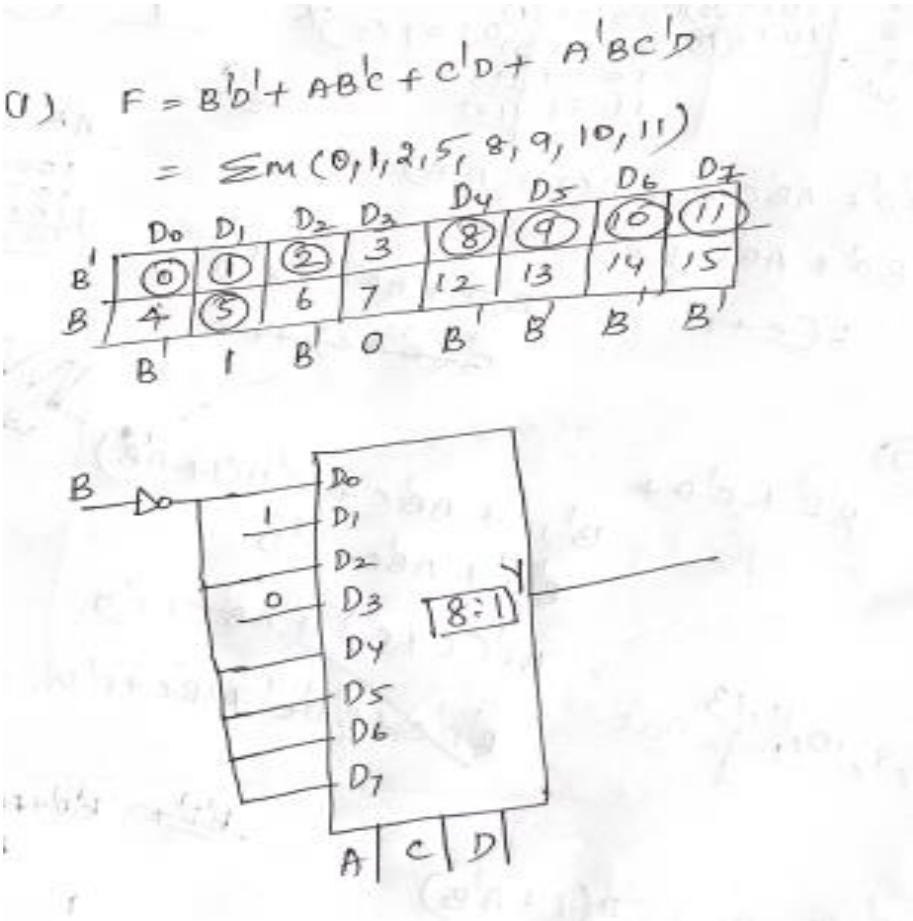
Internal Assesment Test - II

Sub:	**DIGITAL SYSTEM DSESIGN**							Code:	21EE42
Date:	8/08/2023	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	EEE

Answer Any FIVE FULL Questions

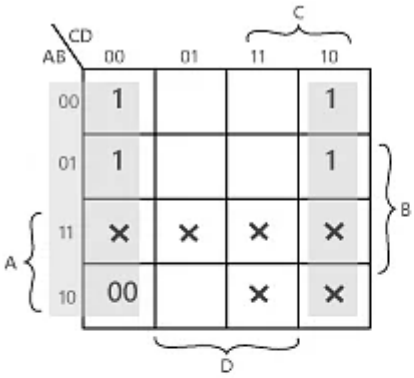
		Marks	OBE	
			CO	RBT
1	Implement the following Boolean function F=B'D'+AB'C+C'D+A'BC'D using a 8:1 MUX with A,C and D as select lines .	10	CO2	L3
2	Design a combinational logic circuit that will convert BCD digit to Excess-3 BCD digit using gates. Construct truth table and simplify the expression using K-maps.	10	CO2	L3
3	Design a 4:16 line decoder by cascading 2:4 line decoder which has active low output and active low enable input.	10	CO2	L2
4	Implement the following Boolean function using a 8:1 MUX with w,y and z as select lines f(w,x,y,z)=Σm(0,1,2,5,7,8,9,12,13)	10	CO2	L3
5	Write the truth table of 2 bit magnitude comparator. Using K-map obtain the expression and represent the same using basic gates	10	CO2	L3
6	What is a Flip-Flop? Discuss the working principal of SR Flip-Flop with the help of truth table.	10	CO3	L2

1.

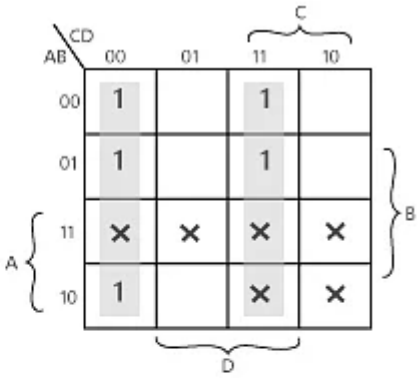


2.

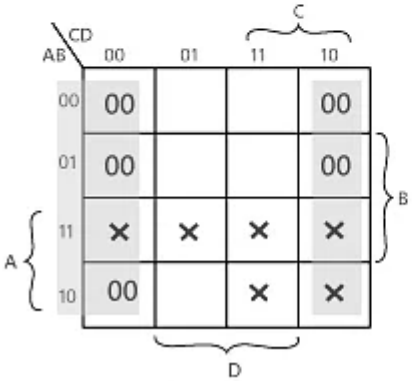
Decimal Number	BCD Code				Excess-3 Code			
	A	B	C	D	W	x	y	z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X



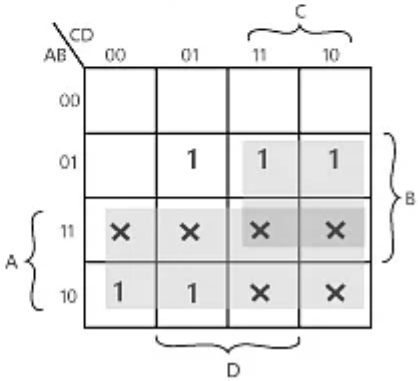
z=D′



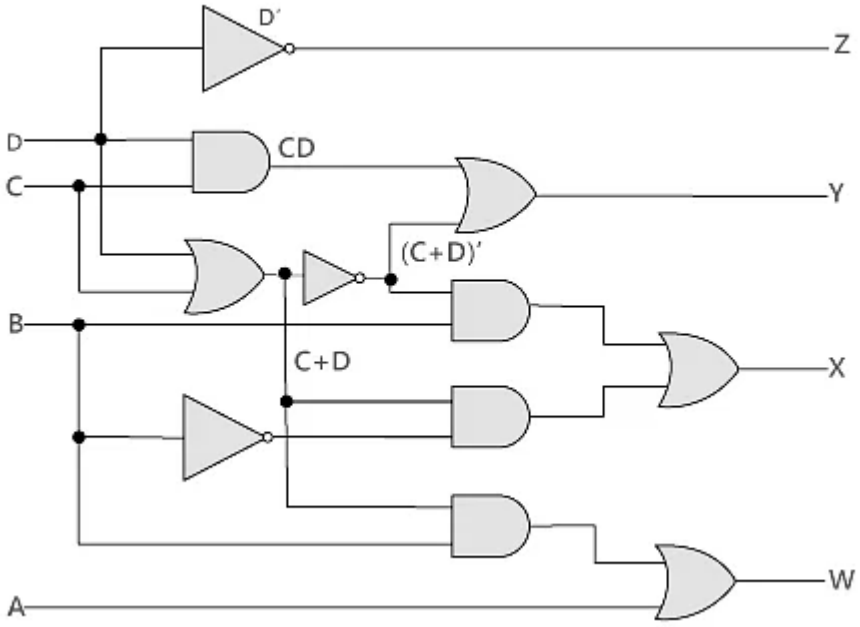
y=CD+C′D′



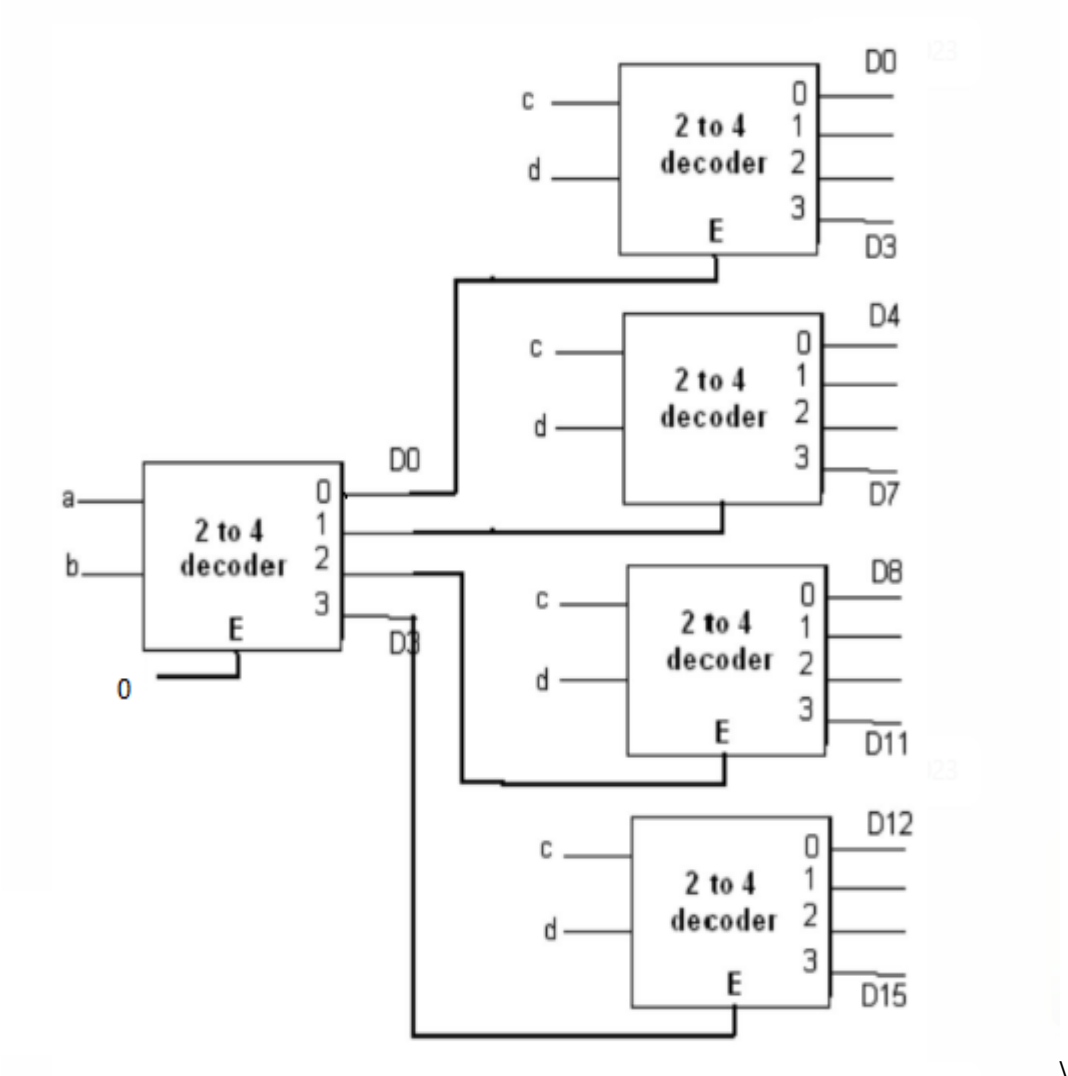
x=B′C+B′D+BC′D′



w=A+BC+BD


D'
Z
D
C
CD
Y
(C+D)'
B
C+D
X
W
A

3.


2 to 4 decoder
E
a
b
0
D0
D3
c
d
D4
D7
D8
D11
D12
D15

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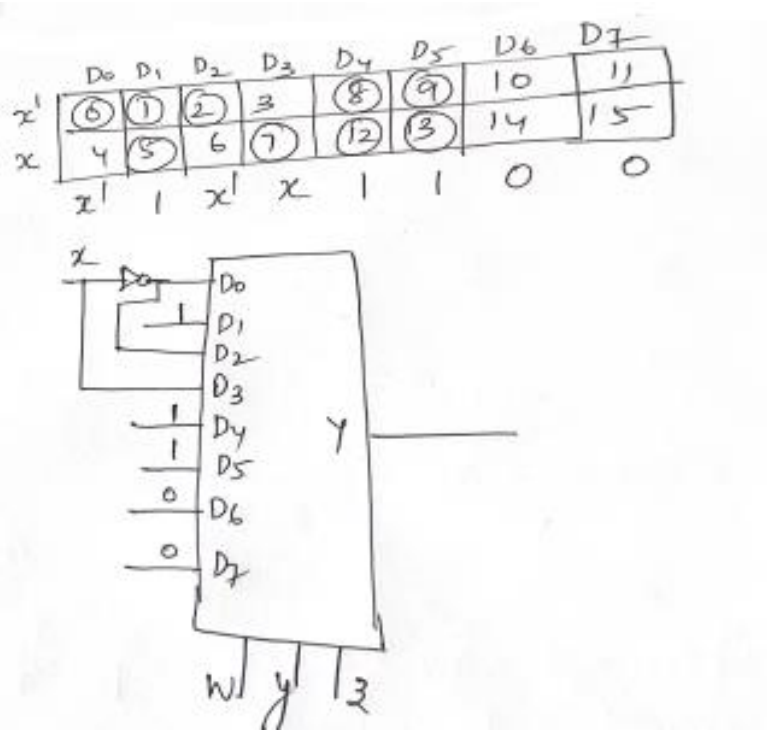
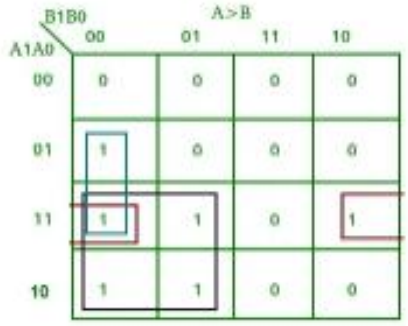
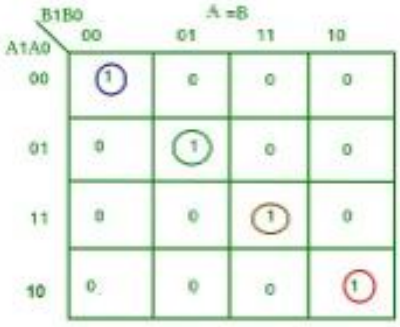
4.



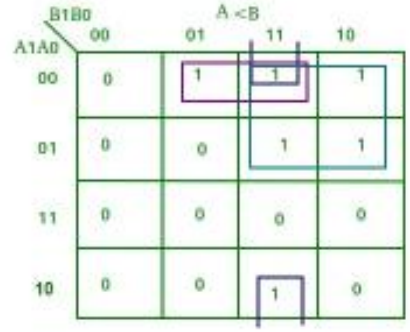
5.

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

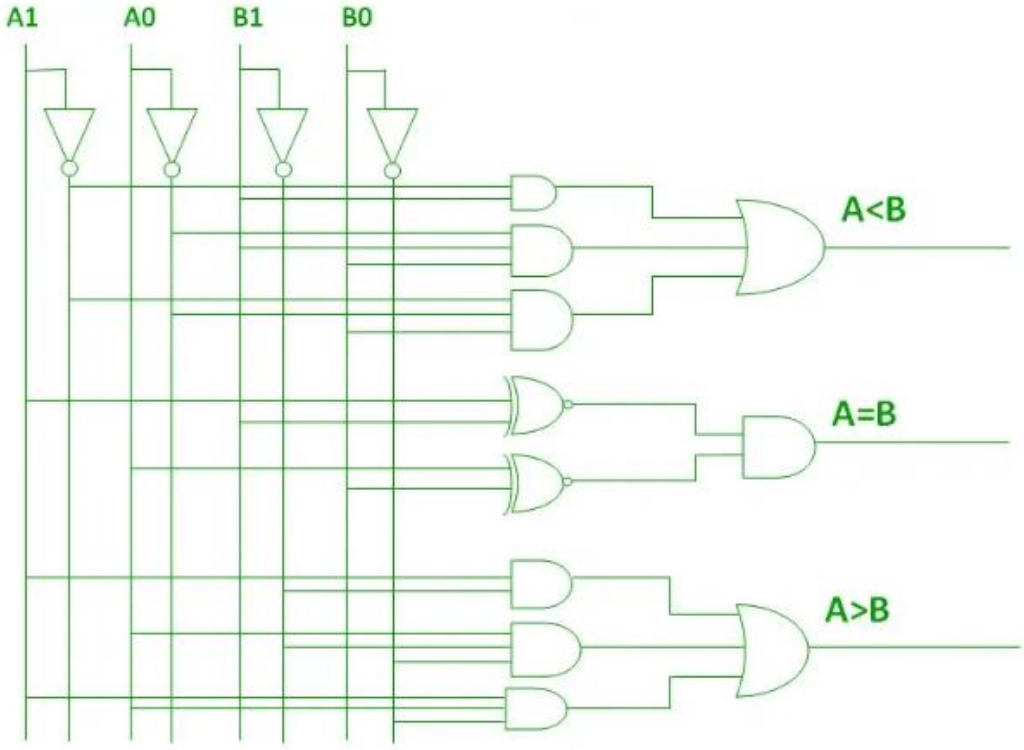




Truth Table of Output A=B




```
A>B:A1B1' + A0B1'B0' + A1A0B0'
A=B: A1'A0'B1'B0' + A1'A0B1'B0 + A1A0B1B0 + A1A0'B1B0'
   : A1'B1' (A0'B0' + A0B0) + A1B1 (A0B0 + A0'B0')
   : (A0B0 + A0'B0') (A1B1 + A1'B1')
   : (A0 Ex-Nor B0) (A1 Ex-Nor B1)
A<B:A1'B1 + A0'B1B0 + A1'A0'B0
```



2-Bit Magnitude Comparator

6.

Flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates.

SR flip-flop is a gated set-reset flip-flop. The S and R inputs control the state of the flip-flop when the clock pulse goes from LOW to HIGH. The flip-flop will not change until the clock pulse is on a rising edge. When both S and R are simultaneously HIGH, it is uncertain whether the outputs will be HIGH or LOW.

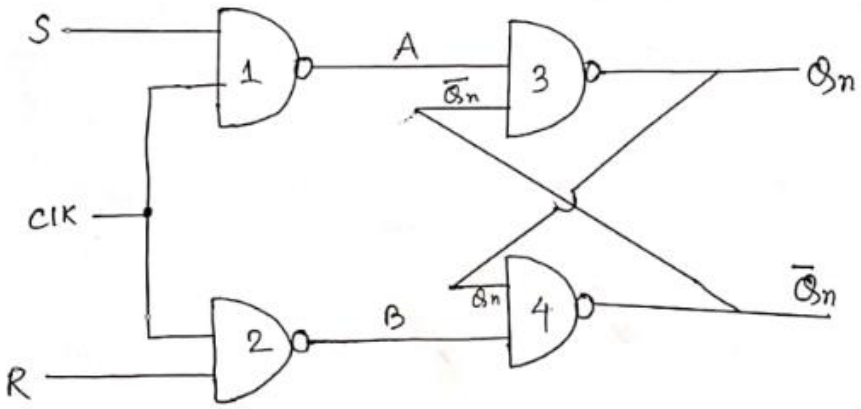
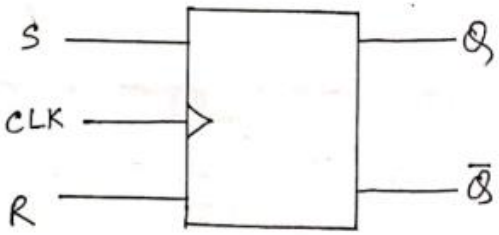


Fig:- Logic Diagram of SR Flip flop.



Truth Table

CIK	S	R	Q_n	Q_{n+1}	State
0	X	X	0	0	No change/ Memory
0	X	X	1	1	
1	0	0	0	0	No change/ Memory
1	0	0	1	1	
1	1	0	0	1	Set
1	1	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	1	0	X	Forbidden
1	1	1	1	X	