CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - III

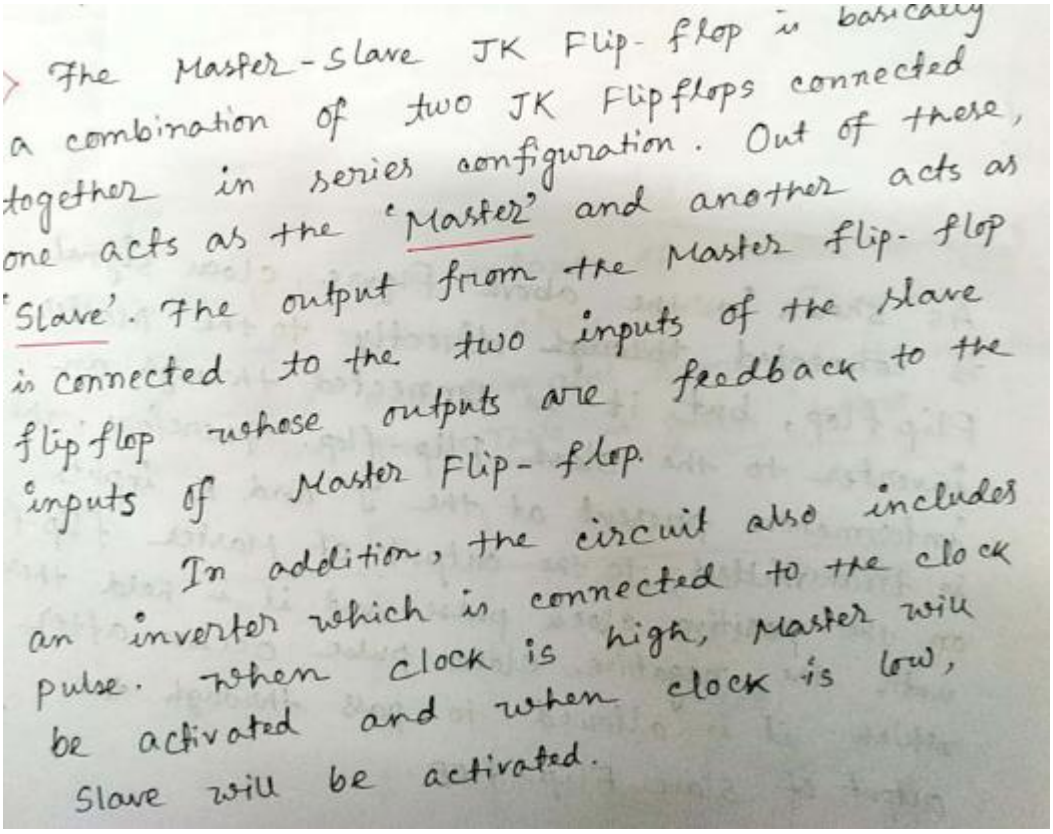
Sub:	DIGITAL SYSTEM DSESIGN							Code:	21EE42
Date:	9/09/2023	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	EEE

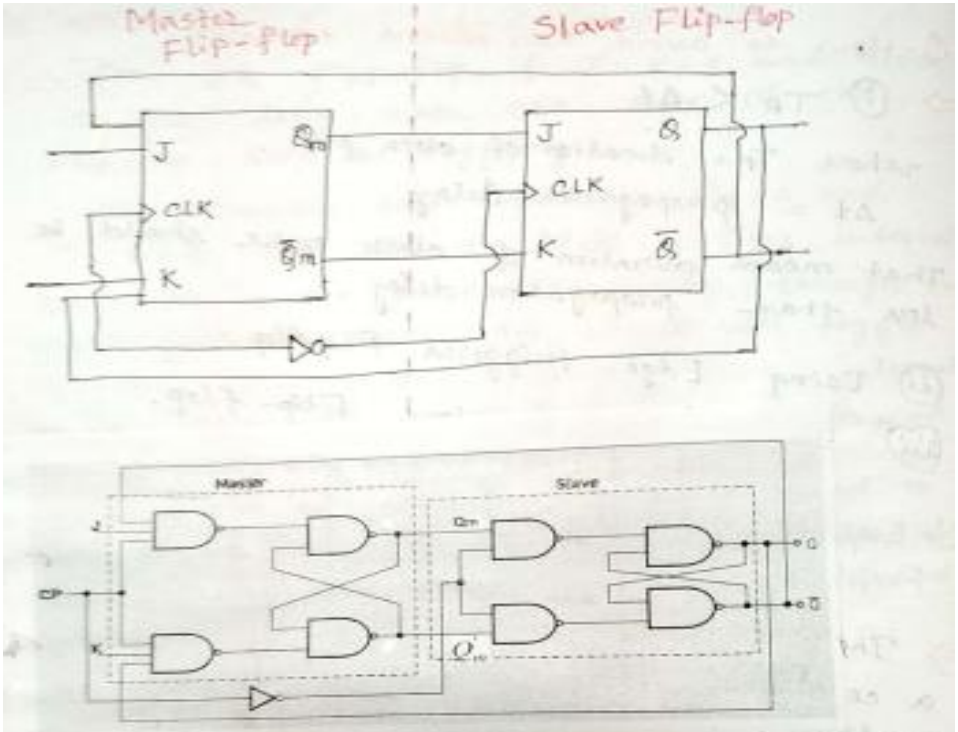
Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Explain the operation of master slave JK Flip-flop along with its circuit diagram	10	CO3	L2
2	Derive the characteristic equations of SR,D,JK and T Flip-flops	10	CO3	L2
3	Draw and explain the working of positive and negative edge triggered D Flip-flop	10	CO3	L2
4	Explain with suitable logic and timing diagram i)Serial in Serial out shift Register ii)Parallel in Parallel out shift Register	10	CO3	L2
5	Design a MOD-5 synchronous binary counter using clocked JK Flip-Flops	10	CO7	L3
6	Compare Registers and counters. Explain the working of 4 bit Asynchronous counter configured using JK Flip-flops	10	CO7	L2

Solutions

1.





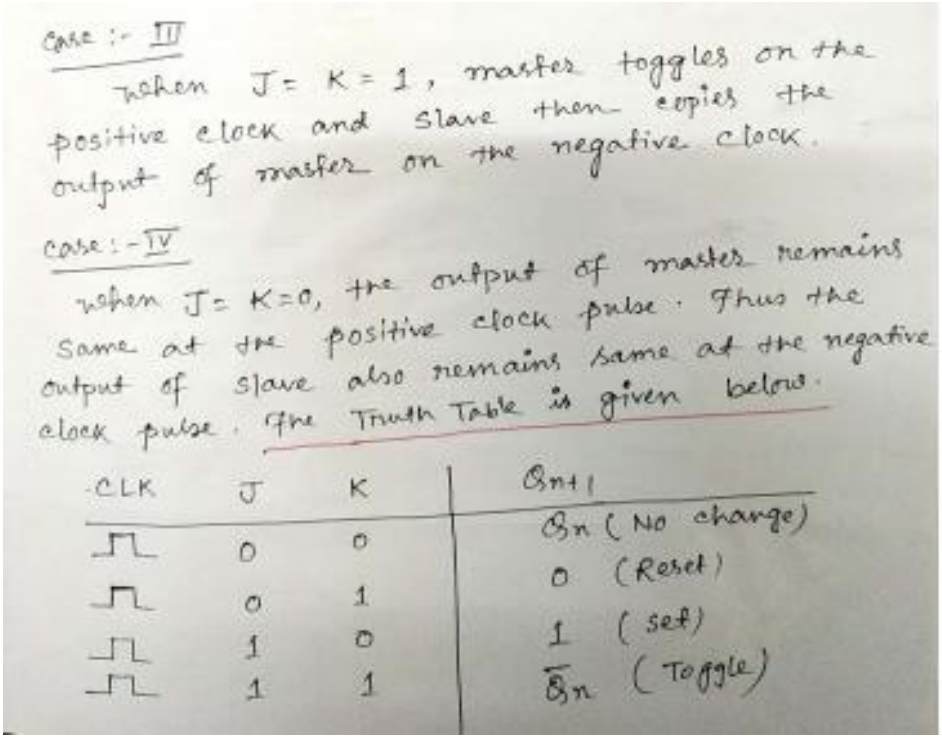
As shown in the above figure, clock signal is connected ~~through~~ directly to the Master Flip flop, but it is connected through an inverter to the slave Flip-flop. Therefore, the information present at the J and K inputs is transmitted to the output of Master flip-flo on the positive clock pulse and it is held there until the negative clock pulse occurs, after which it is allowed to pass through the output of slave Flip-flop.

Case :- I

When J = 1 and K = 0, the Master sets on the positive clock. The high Q_m output of the master drives the J input of the slave, so at negative clock slave sets, copying the action of the Master.

Case :- II

When J = 0 and K = 1, the master resets on the positive clock. The high $\overline{Q}_m$ output of the master goes to the K input of the slave. Thus, at the negative clock slave resets, again copying the action of the master.



2.

SR Flipflop

Truth Table

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Invalid inputs

Characteristic Equation

Q(t+1) = R'(t)Q(t) + S(t) ; S(t)R(t) = 0

Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0

1	0	0	1
1	1	x	0

JK Flipflop

Truth Table

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

Characteristic Equation

$Q(t+1) = K'(t)Q(t) + J(t)Q'(t)$

Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

D Flipflop

Truth Table

D	Q(t+1)
0	0
1	1

Characteristic Equation

$Q(t+1) = D(t)$

Excitation Table

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flipflop

Truth Table

T	Q(t+1)
0	Q(t)
1	Q'(t)

Characteristic Equation

$Q(t+1) = T'(t)Q(t) + T(t)Q'(t) = T(t) \oplus Q(t)$

Excitation Table

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

3.

Positive Edge-Triggered Flip-Flop

The type of edge-triggered flip-flop whose output changes its state only on the rising edge (edge that goes from low to high) of the clock pulse is called a **positive edge-triggered flip-flop**. The positive edge triggered flip flop is also called a **rising edge-triggered flip-flop**. The block diagram of a positive edge triggered flip flop is shown in Figure-3 below.

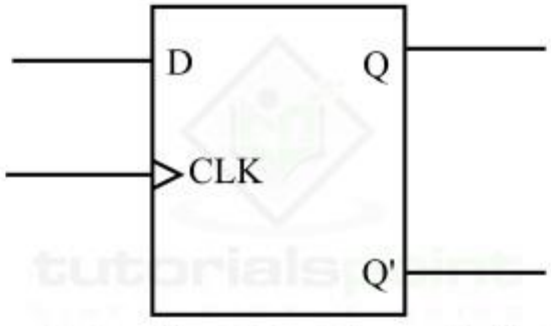


Figure 3 - Positive Edge-Triggered Flip-Flop

In a positive edge triggered flip flop, the inputs are accepted and stored only when the clock pulse goes from low (0) to high (1), i.e. on the rising edge of the clock pulse. This stored value is then available on the outputs.

Negative Edge-Triggered Flip-Flop

The type of edge-triggered flip flop whose output changes its state only on the falling edge (edge that goes from high to low) of the clock pulse is called **a negative edge-triggered flip-flop**. The negative edge triggered flip flop is also known as a **falling edge-triggered flip-flop**. The block diagram of a negative edge triggered flip flop is shown in Figure-4 below.

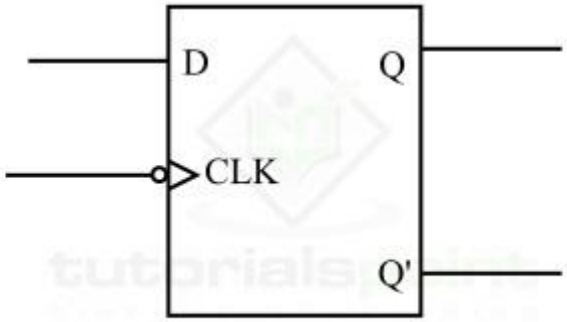


Figure 4 - Negative Edge-Triggered Flip-Flop

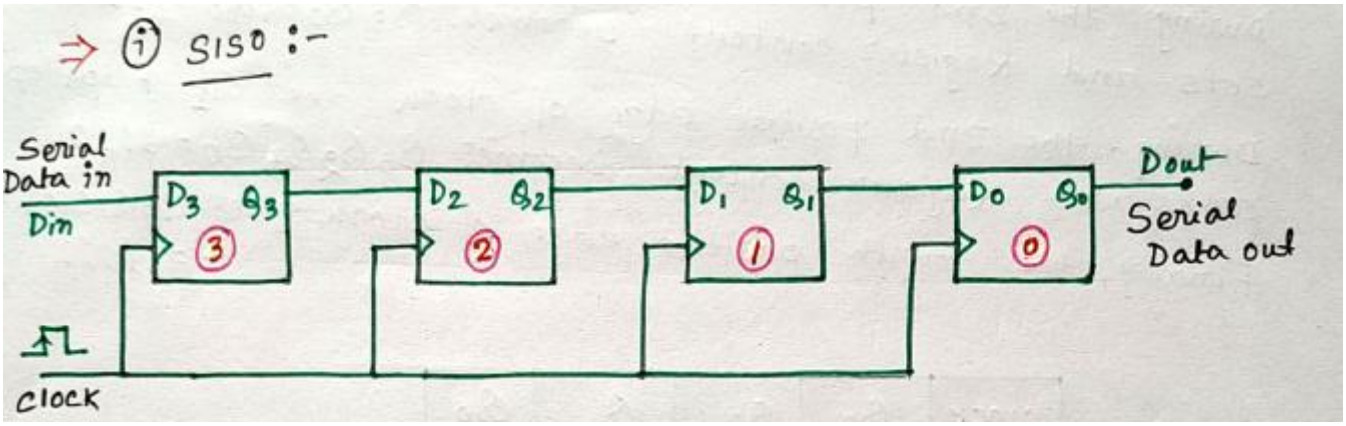
In the case of negative edge triggered flip flop, the flip-flop captures and stores the inputs only when the clock pulse goes from high to low, i.e. on falling edge of the clock pulse.

Operation of Edge-Triggered Flip-Flop

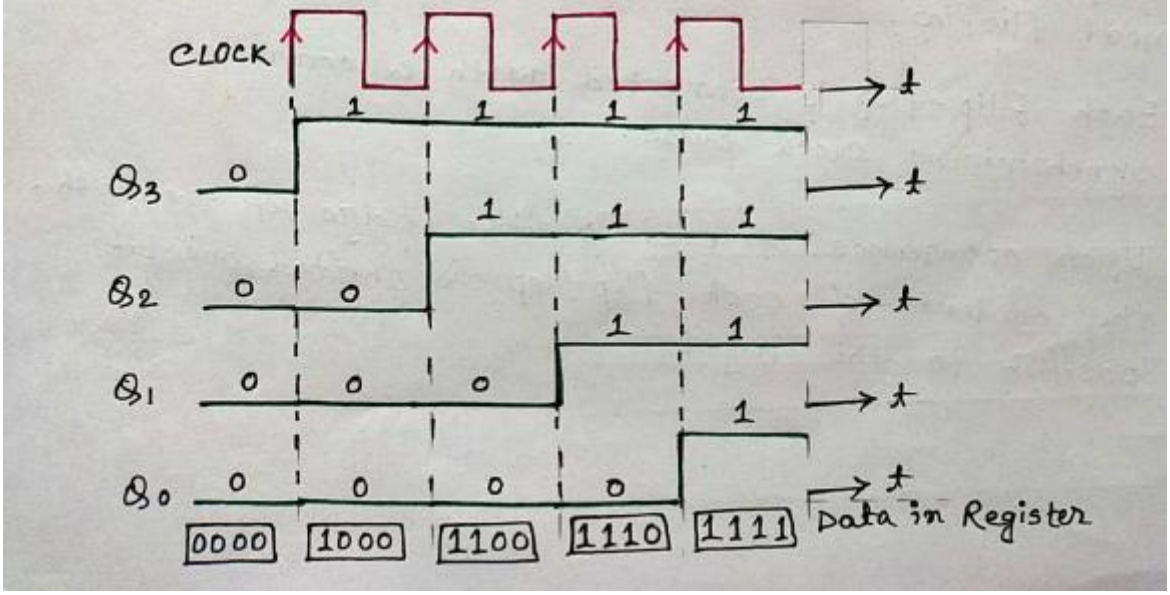
The operation of a typical edge-triggered flip-flop is described below −

In the edge-triggered flip-flop, the inputs are applied through the input terminals and a clock pulse is connected to the clock input of the flip-flop. The edge triggered flip flop responds according to the applied inputs when the clock pulse goes from either low to high or high to low. When this state transition of clock pulse occurs, the flip-flop captures and stores the input values. These stored input values will be then available on the outputs (Q and Q') of the flip-flop.

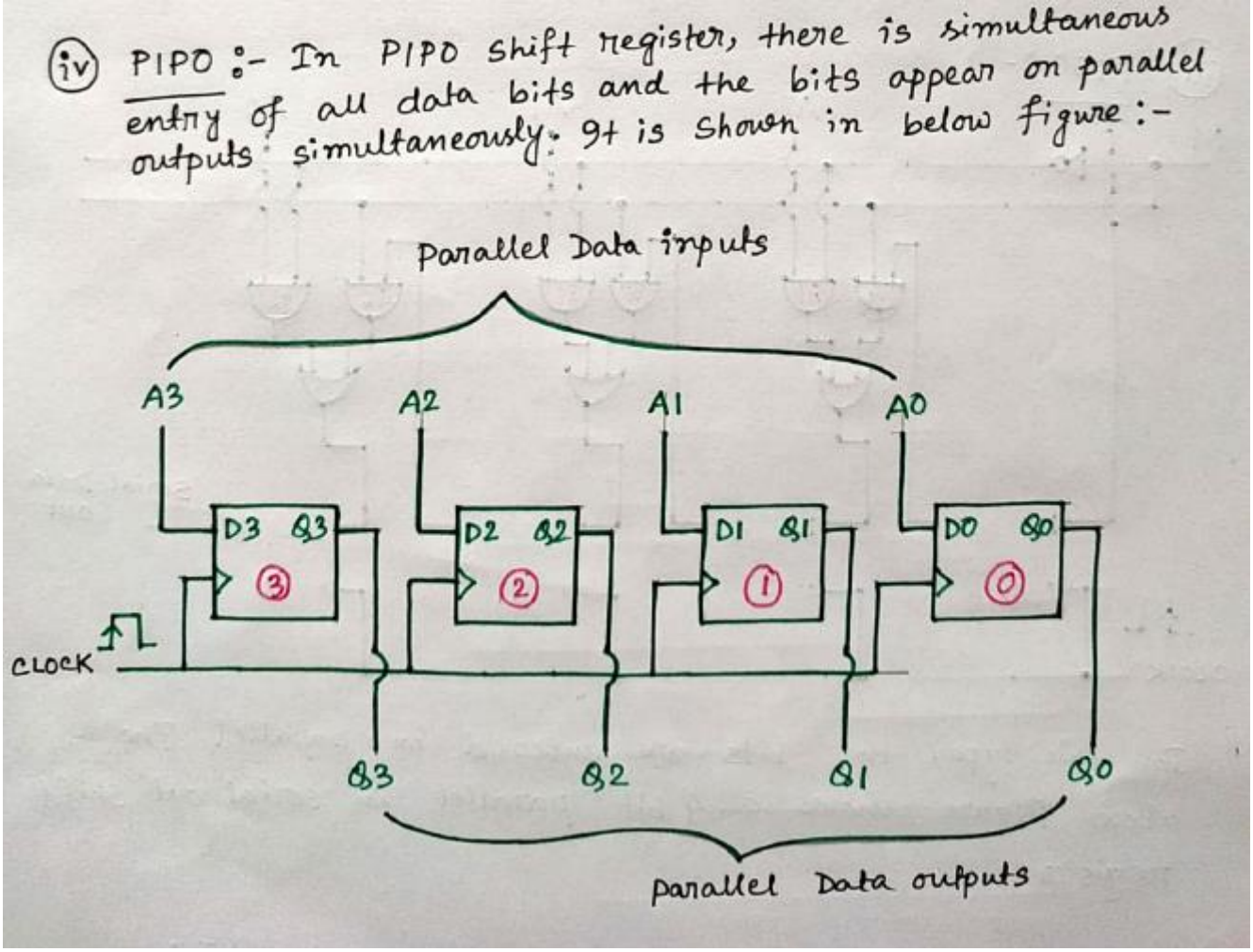
4.



CLOCK	Q_3	Q_2	Q_1	Q_0
–	0	0	0	0
1↑	1	0	0	0
2↑	1	1	0	0
3↑	1	1	1	0
4↑	1	1	1	1



(iv) PIPO :- In PIPO shift register, there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously. It is shown in below figure :-



5.

1) Excitation table for JK flip flop

Q_n	Q_{n+1}	**J**	**K**
0	0	0	×
0	1	1	×
1	0	×	1

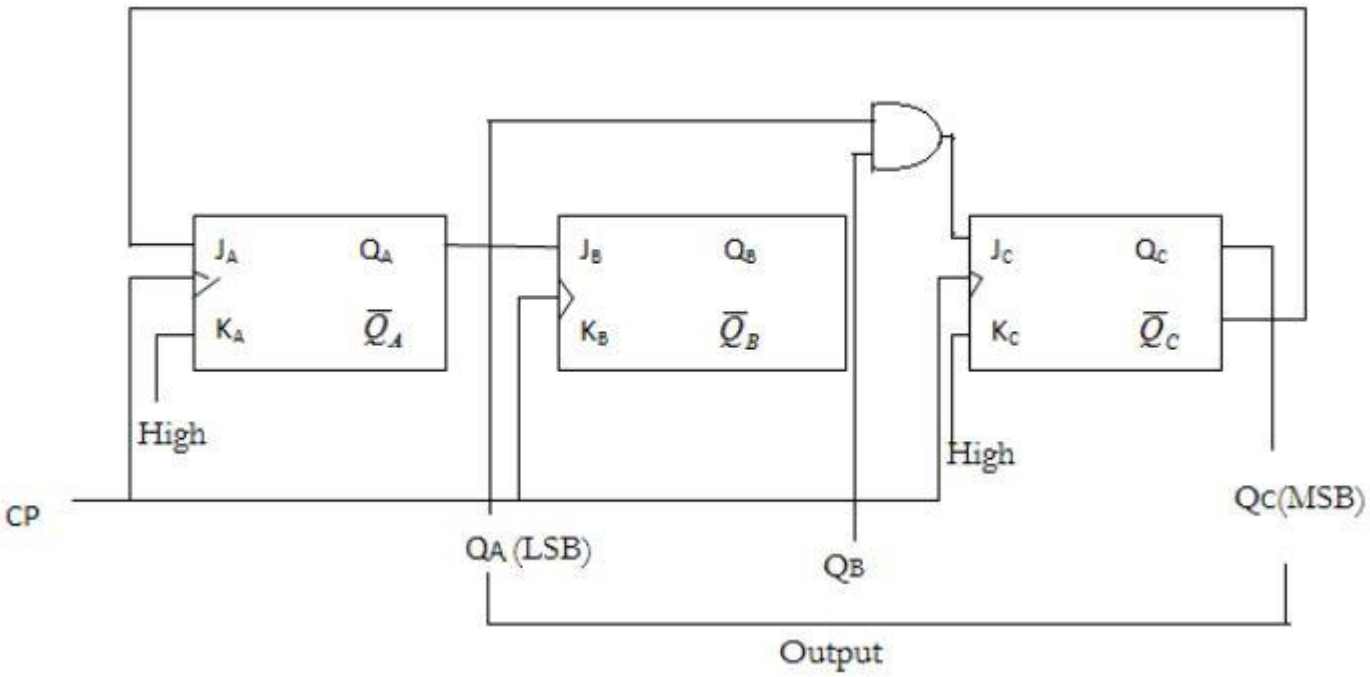
Now, we can derive excitation table for counter using above table as follows:

2) Excitation table for counter

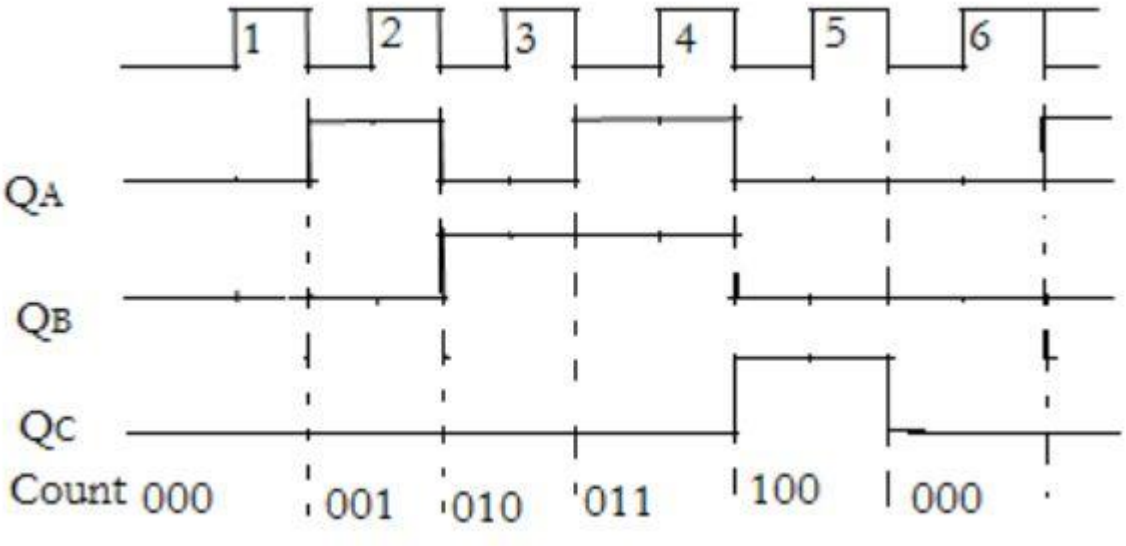
Present state			Next state			Flip flop Input					
Q_c	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_a
0	0	0	0	0	1	×	0	0	×	1	×
0	0	1	0	1	0	×	1	1	×	×	1
0	1	0	0	1	1	×	×	×	0	1	×
0	1	1	1	0	0	×	×	×	1	×	1
1	0	0	0	0	0	1	0	0	×	0	×
1	0	1	×	×	×	×	×	×	×	×	×
1	1	0	×	×	×	×	×	×	×	×	×
1	1	1	×	×	×	×	×	×	×	×	×

$J_C=Q_BQ_A$ $K_C=1$ $J_B=QA$ $K_B=QA$ $J_A=Q_C'$ $K_A=1$

Step 5 Logic Diagram



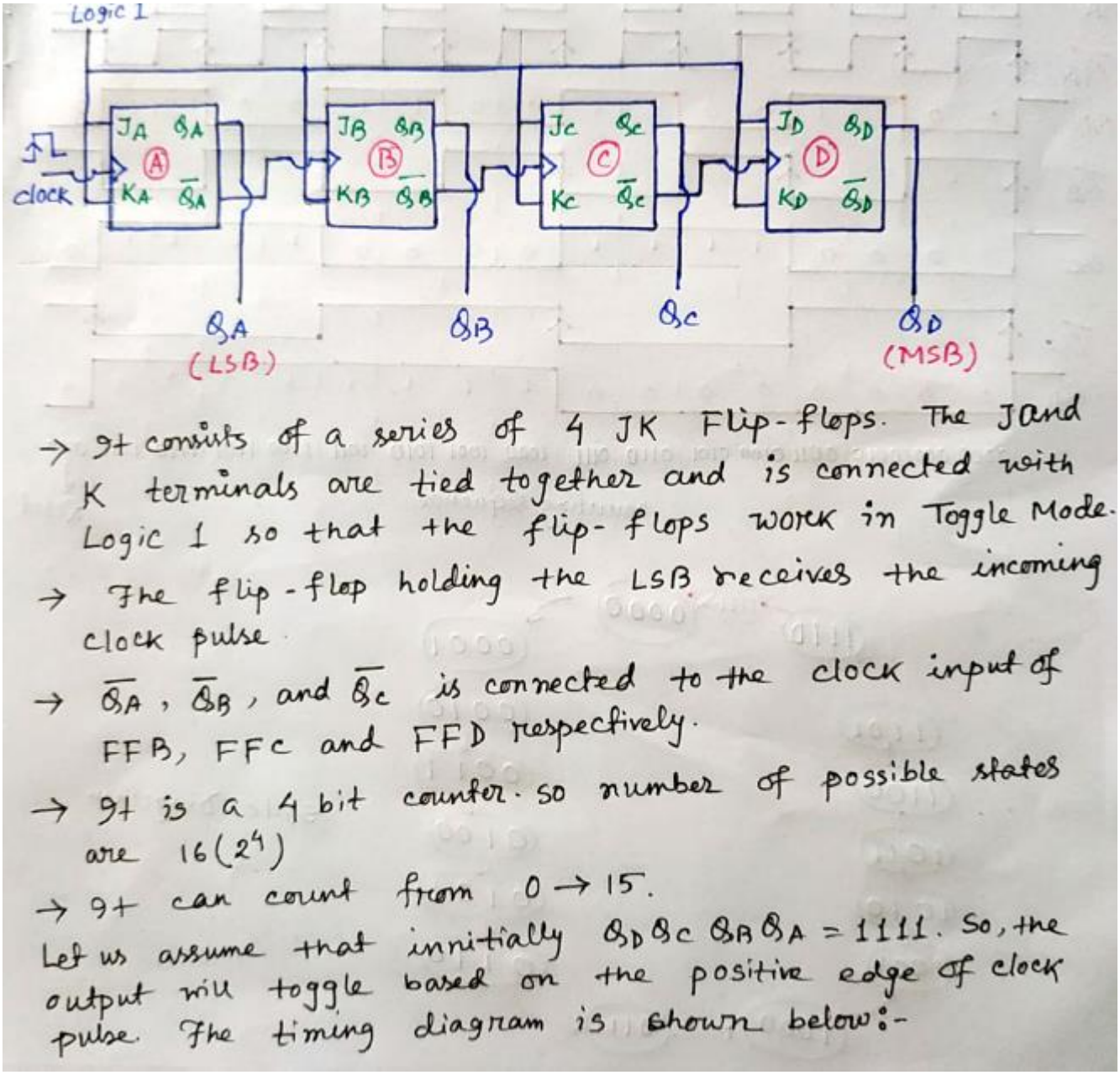
Step 6: Timing Diagram



6.

Register	Counter
Register can hold data to use as a temporary memory storage	Counter can only be loaded, stored or incremented as a program counter

It does not follow specific sequence of states	Follow specific sequence of states
It has the same clock	It does not need a same clock
Its path of stage is not predefined	Its path of stage is predefined
All register is not counter	All counter is register



→ It consists of a series of 4 JK Flip-flops. The J and K terminals are tied together and is connected with Logic 1 so that the flip-flops work in Toggle Mode.

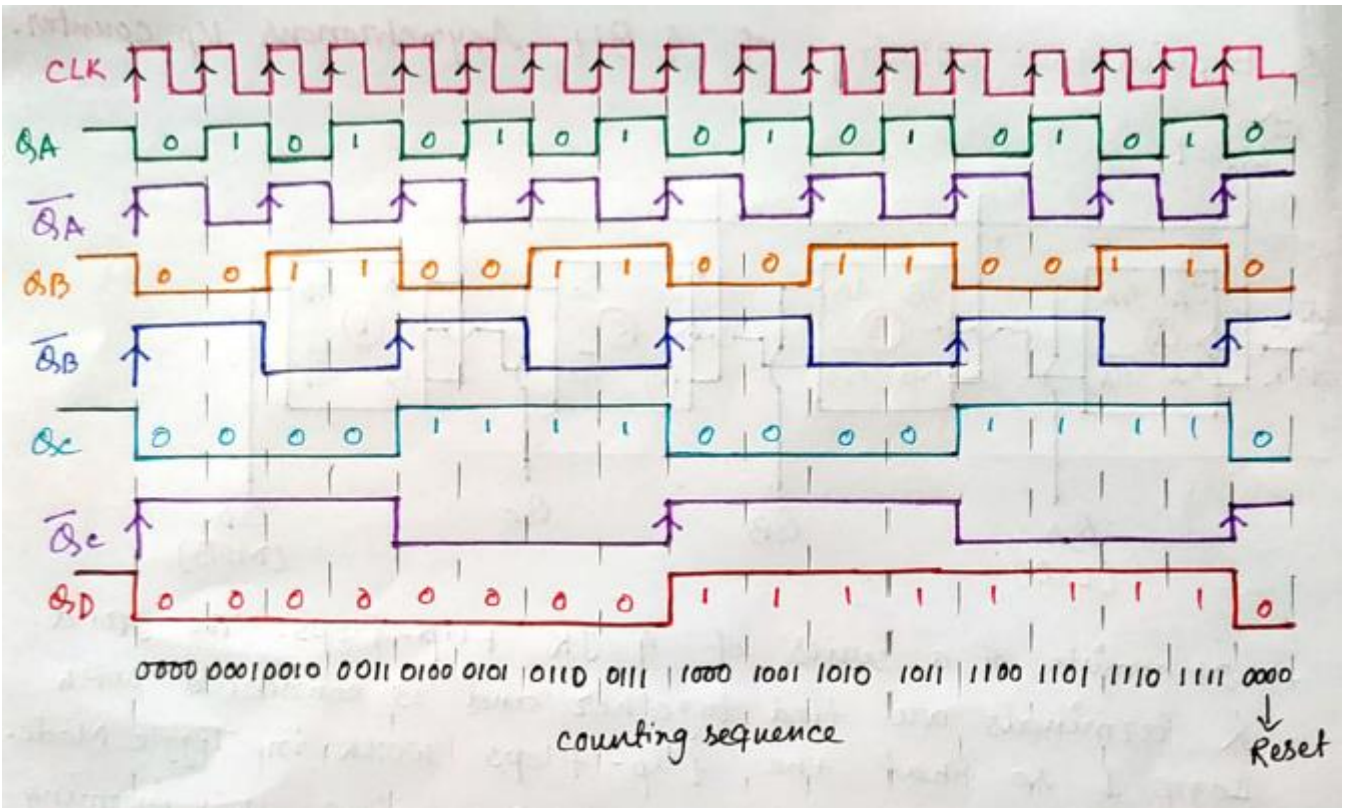
→ The flip-flop holding the LSB receives the incoming clock pulse.

→ $\overline{Q_A}$, $\overline{Q_B}$, and $\overline{Q_c}$ is connected to the clock input of FFB, FFC and FFD respectively.

→ It is a 4 bit counter. So number of possible states are 16 (2^4)

→ It can count from 0 → 15.

Let us assume that innitially $Q_D Q_C Q_B Q_A = 1111$. So, the output will toggle based on the positive edge of clock pulse. The timing diagram is shown below:-


CLK
QA
$\overline{Q_A}$
QB
$\overline{Q_B}$
Qc
$\overline{Q_c}$
QD
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000
counting sequence
Reset