There are 13 General purpose registers in Cortex M3 processor

- R_0 - R_{12} are general purpose registers. When a 16 bit thumb instruction calls a register only the subset of the registers (R_0 - R_7) is used.
- R_{13} is a stack pointer. There are 2 stack pointers banked together in Cortex M3. At a given time only one stack pointer is accessable.

Main stack pointer : It is a default stack pointer. It is used for operating interrupt handlers.

Process stack pointer : It is user defined stack pointer

- R_{14} is the link register. Whenever a subroutine is called the return address of the main program is stored in link register.
- R_{15} is the Program Control which stores the address of the next instruction to be executed.

R_0
R_1
R_2
R_3
R_4
R_5
R_6
R_7 — Low level — General Purpose registers
R_8
R_9
R_{10} — High level
R_{11}
R_{12}

The Special Purpose registers in Cortex M3 are.

1) Program Status Register
2) Interrupt Mask Register
3) Control Register.

1) Program Status Register:

There are 3 PSRs,

i) Application Program Status register.
ii) Interrupt Program Status register
iii) Exception Program Status register

All the 3 PSRs can be accessed together or individually. When they are to be accessed together xPSR is used. The Instructions MSR & MRS can be used to Write & Read the PSRs.

APSR, IPSR, EPSR can be read using MRS Instruction
But only APSR can be written using MSR Instruction

eg:

```
MRS  R0, APSR
MRS  R0, IPSR
MRS  R0, EPSR
MSR  R0, APSR.
```

	31	30	29	28	27	26-25	24	23-20	19-16	15-10	9-0
APSR	N	Z	C	V	Q						
IPSR											Exception no.
EPSR						ICI IT	T				

Accessing of Bits by PSR.

	31	30	29	28	27	26-25	24	23-20	19-16	15-10	9-0
XPSR	N	Z	C	V	Q	ICI IT	T				Exception no.

N → Negative number
Z → Zero
C → Carry / Borrow
V → Overflow
Q → Sticky Saturation bit
ICI → Interrupt Continuable Instruction
T → Thumb
Exception → an exception number.

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9) Interrupt Mask registers

There are 3 IMR's

BASERI, FAULTPRI, PRIMASK.

BasePRI & PRIMASK are helpful in masking the Interrupts during unfavourable conditions

FAULTMASK mask the interrupts when there is fault.

BASEPRI : It is a 1 bit register. It is always set to 0. Whenever it is set to 1. it masks the all the interrupts allowing only Non maskable Interrupts & hard fault exceptions. Default it is zero.

PM
PRI

FAULTMASK : It is a one bit register. It mask only fault handler interrupt exception & allows all other interrupts including NMI. By default is 0.

BASEPRI : It is a 8 bit register. It is used for priority masking. It mask all low level priority interrupts. By default is 0.

3) Control register:

There are 2 control registers 'control[1]' & control[0].

control[1]: It is always zero in thread mode. It can be either zero or one in the handler mode.

It can be written only in handler & privilaged mode. If we have to change it we can access the bit 2 of the link register.

control[0]: It can be written only in the privilaged mode. If we have to change it we have to interrupt it by calling a interrupt through exception handler.

2) Applications:

1) Low cost microcontrollers:

The Cortex M3 is ideally suited for low cost microcontrollers & can be used for wide range of consumer products from toys to electrical appliances. The market is wide & highly popular due to development of 8 bit & 16 bit microcontrollers.

2) Automotive:

Ideally Cortex M3 is suitable for wide range of automotive applications. Due to the properties of high efficiency, low power consumption & low interrupt latency. it can be used in automotives.

3) Data communication:

The properties such as simplicity, reliability and ease of use make data process to occur at least range. The flexibility of Cortex M3 & ability of interrupt communication makes it fit for the bluetooth & zigbee communications.

4) Industrial Control:

The properties such as high efficiency, low power consumption, low interrupt latency, makes Cortex M3 an important part of Industrial control

5) Consumer products:

The microprocessor Cortex M3 can be used in wide range Consumer products due to its efficient performance & low interrupt latency.

4) Exceptions and Interrupts:

The exceptions can be programmable or non programmable during a task performance.

Whenever an Interrupt is called the processor stops the currently executing task to performs the interrupt service routine

The priorities can be explained by the below table

Exception no.	Exception name	Priority	Function
1	Reset	-3	Reset
2	NMI	-2	Non Maskable Interrupt
3	HardFault	-1	Blocks the faults.
4	Mem Manage fault	Settable	Memory Management fault.
5	Bus fault	Settable	Error during procesing a Bus.
6	Usage fault	Settable	Instruction error is resolved
7 - 12	-	-	Reserved
13	SVC	Settable	Vector Call.
14	Debug monitor	Settable	Debug Monitoring.
15	-	-	Reserved.

15	PendSV	Settable	Pendable Service is resolved by Servicing
16	Systick	Settable	System tick timer
17	IRQ	-	IRQ bits #0 - 239
255			

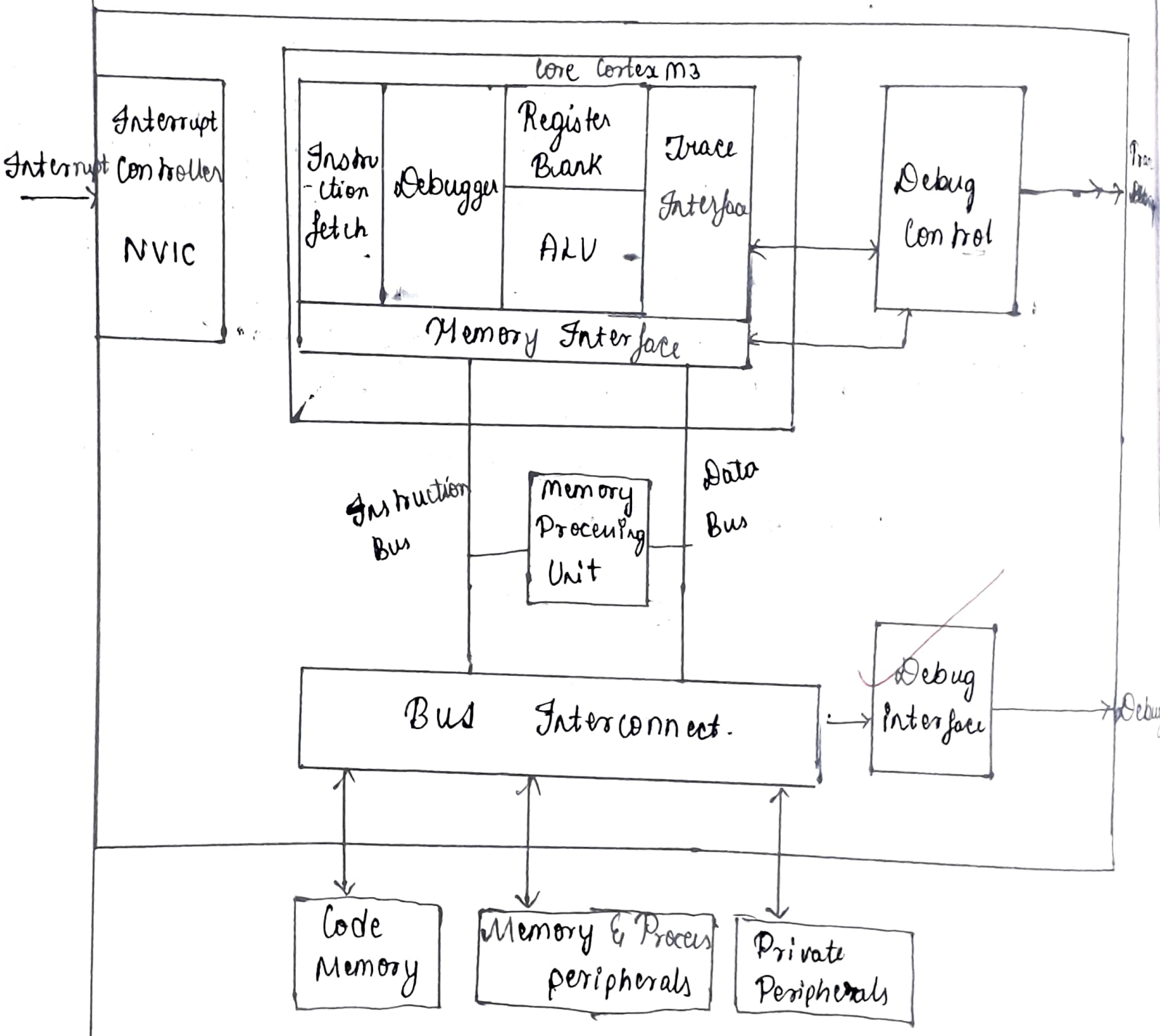
Vector Table

Exception address	Exception	Function
0x 00000000	-	MRS start value
0x 00000004	Reset	Reset Starting add
0x 00000008	NMI	NMI Stating add
0x 0000000A	Hardfault	Hardfault Starting ad
0x 0000000D	—	Other Interrupt Starti address

Vector Table & Priority table provides a breif information about the interrupt being Servied & exceptions being handled whenever they are called.

The priorities are set to perform the actions in a suitable manner with proper steps.

~~address~~ data path, 32 bit register bank & 32 bit memory interface. It has Hordvard architecture. The data & Instruction can be processed at the same time. This increases the speed of the processor as the data fetch do not interfere the Instruction pipelining. Hence multiple Bus Interface can be done.



* The Cortex M3 consists of 13 General purpose registers [R0-R12] 2 stack pointers (MSP, PSP) [R13], one link register [R14], one program counter [R15] & special purpose registers including PSR.

* The Cortex M3 core consists of a Debugger with Traditional thumb with additional thumb instructions and an ALU to support the hardware multiply, divide and connect to the other ports & peripherals.

* The NVIC is an integral part of the Cortex M3 since it's function in servicing the Interrupts & resolving interrupt handling problems

* The Cortex M3 is a single memory mapped device with a fixed single memory of 4 Gigabytes. to the code, SRAM, internal / external interrupts, external devices.

* The MPU is an optional component of the Cortex M3, It provides safeguarding of memory. & protects the data from the Operating System during application development.

* The instruction & data Bus communicates with the memory & provides help in fetching the data & the Instruction

* The Non Maskable Interrupt has a wide range of application as it provides help during the masking of interrupts in unfavorable conditions.

* The debug can be accessed via a debug port. to find the solutions regarding the malfunctioning of any components of the Cortex M3.

6) The Cortex M3 addresses the 32 bit processor in the following ways.

* Improved Performance efficiency:
  Large work done with the use of lower frequency & less power consumption
* Low Power consumption:
  The efficiency is increased as a result ensuring there is less power consumed.
* Enhanced Determinism:
  Ensuring that all the interrupts called are serviced as quick as possible with known number of cycles.
* Increased Code Density:
  Enabling the processor to store the code within the memory requirements provided.
* Ease of Use:
  Providing the requirements to be satisfied by the 32 bit processor similar to that of 16 bit & 8 bit processor so that the consumer can easily shift into the system.
* Low Cost Solutions:
  Providing a reliable cost solution to the user. Similar to that of 8 bit & 16 bit.