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Department of AI-ML and AI-DS Internal Assessment Test 3 – September 2023

Sub:	Microcontrolle	r & Embedded	d Systems			Sub Code:	21CS43	Branc	ch: AI-	ML & A	I-DS	
Date:	09-09-23	Duration:	90 min's	Max Marks:	50	Sem / Sec:		4 th		OBE		
		An	swer any FI	VE FULL Quest	tions				MARKS	CO	RBT	
1.	Write a short note on utility of LED and Seven segment display as actuators								[10]	CO4	L3	
2.	Discuss the ar	Discuss the architecture and working of Inter Integrated Circuit or I2C or I ² C protocol							[10]	CO4	L3	
3.	Explain the co	onstruction a	nd working o	of Reset and Br	owno	out protection	n circuit.		[10]	CO4	L3	
4.	Discuss in det	ail about the	OS architec	ture for RTOS	basec	l embedded s	system design		[10]	CO5	L2	
5.	Elaborate the	Elaborate the functions of the Real-Time Kernel							[10]	CO5	L2	
6.	Explain the concept of Mailbox and the Sockets for IPC						[10]	CO5	L2			
7.	Define Deadlock. Explain the Racing conditions due to deadlock and methods to handle deadlock					ndle	[10]	CO5	L3			

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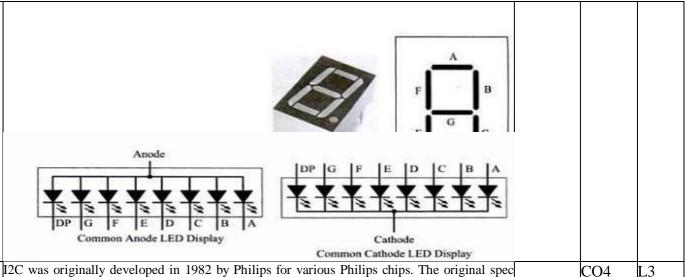
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Internal Assessment Test 3 – September 2023

nterna	l Assessment Te	est 3 – Septen	iber 2023			1	I		1		
Sub:	Microcontrol	ler & Embedd	led Systems			Sub Code:	21CS43	Branch:	AI-ML & AI-		
ate:	09-09-23	Duration:	90 Minutes	Max Marks:	50	Sem / Sec:	4 th		OBE		
G 1	1014							MADIZO	CO	DDT	
Schen 1	ne and Solution	unction diode	and contains a	CATHODE and	ANO	DE For function	oning the and	MARKS	CO CO4	RBT L3	
	is connected to The maximum	+ve end of po	ower supply an ing through th	d cathode is core LED is limit s shown in the f	nnected ed by	l to -ve end o connecting a	f power supp	ly.			
						^V CCC	DD .				
	There are two v	ways to interfa	ace an LED to a	microprocesso	r/micro	ocontroller:					
			_	ort pin and cathon it is at logic h			is approach t	the			
	r -	s the current	to the LED who	port pin and A en it is at logic the port pin is a	high (e. 1). Here th					
	displays. Seven- calculators, and The seven elen numerals. Ofte aids readability (usually elonga case of adding an effort to fu different glyph has two versior The seven segre horizontal segre the rectangle h	laying decimal- segment displayed of the deciron nents of the deciron nents of the deciron nents applayed hexagons machines, the of the results on seven-seas, with or with the nents are arranged to orizontally. The segment of the corizontally.	al numerals that blays are widel nic devices that isplay can be legments are an lications, the set, though trapeze vertical segment ereadability. The gment displays hout segment Finged as a rectar op, middle, and there are also	t is an alternative used in digital display numeriate in different corranged in an observen segments about and rectangents are longer and an enumerals 6, with or without [4] angle of two vert bottom. Addition fourteen-segments	ve to tal clo ical information blique are of r gles ca and mor and 9 ut a 'tal ical se onally ient	the more completes, electronic committees, el	sent the Aral agement, whi shape and si o, though in the dat the ends esented by two numeral 7 all the side with o segment bised sixteen-segment.	rix sic bic ich ize the in wo lso one cts ent			
	displays (for fi displays. Twen were briefly a segment displa	ull alphanum ty-two segme vailable in th y are referred	erics); however ent displays cap e early 1980s, I to by the lett	these have modele of display but did not press A to G, where the display	ostly ing the overpose the	been replaced e full ASCII opular.The se e optional de	by dot mate character set gments of a cimal point (rix [5] 7-			

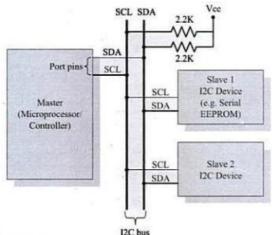


I2C was originally developed in 1982 by Philips for various Philips chips. The original spec allowed for only 100kHz communications, and provided only for 7-bit addresses, limiting the 10 number of devices on the bus to 112 (there are several reserved addresses, which will never be used for valid I2C addresses). In 1992, the first public specification was published, adding a 400kHz fast-mode as well as an expanded 10-bit address space. Much of the time (for instance, in the ATMega328 device on many Arduino-compatible boards), device support for I2C ends at this point. There are three additional modes specified: fast-mode plus, at 1MHz; high-speed mode, at 3.4MHz; and ultra-fast mode, at 5MHz.

2

Each I2C bus consists of two signals: SCL and SDA. SCL is the clock signal, and SDA is the data signal. The clock signal is always generated by the current bus master; some slave devices may force the clock low at times to delay the master sending more data (or to require more time to prepare data before the master attempts to clock it out). This is called "clock stretching" and is described on the protocol page.

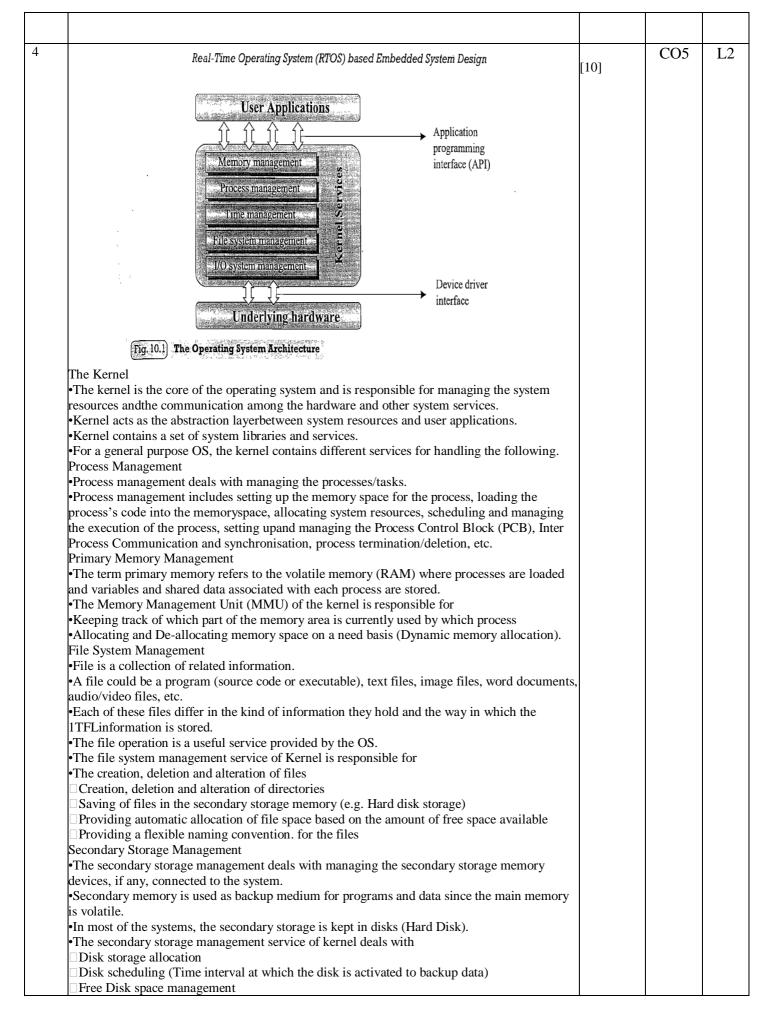
Unlike UART or SPI connections, the I2C bus drivers are "open drain", meaning that they can pull the corresponding signal line low, but cannot drive it high. Thus, there can be no bus contention where one device is trying to drive the line high while another tries to pull it low, eliminating the potential for damage to the drivers or excessive power dissipation in the system. Each signal line has a pull-up resistor on it, to restore the signal to high when no device is asserting it low.



The sequence of operation for communicating with an I2C slave device is:

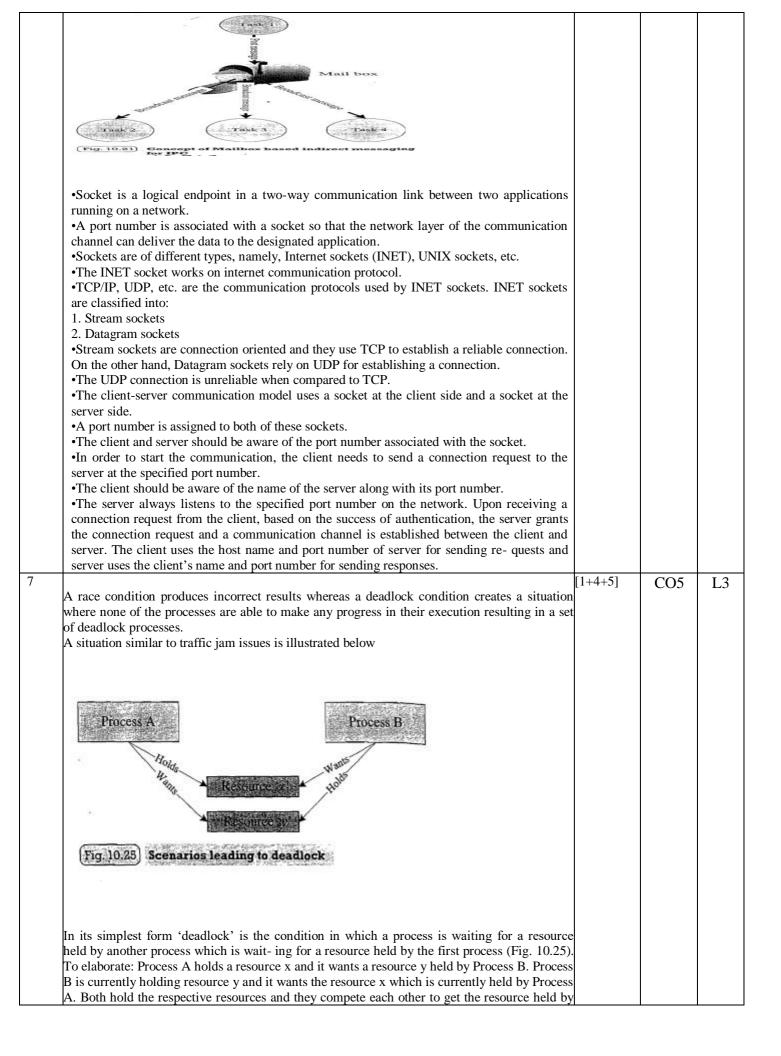
- 1. Master device pulls the clock line (SCL) of the bus to 'HIGH'
- 2.Master device pulls the data line (SDA) 'LOW', when the SCL line is at logic 'HIGH' (This is the 'Start' condition for data transfer)
- 3.Master sends the address (7 bit or 10 bit wide) of the 'Slave' device to which it wants to communicate, over the SDA line. Clock pulses are generated at the SCL line for synchronizing the bit reception by the slave device. The MSB of the data is always transmitted first. The data in the bus is valid during the 'HIGH' period of the clock signal
- 4.Master sends the Read or Write bit (Bit value = 1 Read Operation; Bit value = 0 Write Operation) according to the requirement
- 5.Master waits for the acknowledgement bit from the slave device whose address is sent on the bus along with the Read/Write operation command. Slave devices connected to the bus compares the address received with the address assigned to them

·				
	6. The Slave device with the address requested by the master device responds by sending an			
	acknowledge bit (Bit value =1) over the SDA line			
	7. Upon receiving the acknowledge bit, master sends the 8bit data to the slave device over			
	SDA line, if the requested operation is 'Write to device'. If the requested operation is 'Read			
	from device', the slave device sends data to the master over the SDA line			
	8.Master waits for the acknowledgement bit from the device upon byte transfer complete for a			
	write operation and sends an acknowledge bit to the slave device for a read operation			
	9.Master terminates the transfer by pulling the SDA line 'HIGH' when the clock line SCL is at			
	logic 'HIGH' (Indicating the 'STOP' condition)			
3	Reset circuit:		CO4	L3
		10	201	L 3
	where the device is not guaranteed to operate, during system power ON. The Reset signal			
	brings the internal registers and the different hardware systems of the processor/controller to			
	a known state and starts the firmware execution from the reset vector (Normally from vector			
	address 0x0000 for conventional processors/controllers. The reset vector can be relocated to			
	an address for processors/controllers supporting bootloader			
	The reset signal can be either active high (The processor undergoes reset when the reset pin			
	of the processor is at logic high) or active low (The processor undergoes reset when the reset			
	pin of the processor is at logic low).			
	• Vcc • Vcc			
	± ± ± ± ±			
	-T ^C Reset pulse			
	Reset pulse Active high Reset pulse			
	Reset pulse			
	Active high Reset pulse Active low			
	#			
	E CND			
	GND JGND			
	W. Control of the Con			
	Brownout Protection			
	Brown-out protection circuit prevents the processor/controller from unexpected program			
	execution behavior when the supply voltage to the processor/controller falls below a			
	specified voltage. The processor behavior may not be predictable if the supply voltage falls			
	below the recommended operating voltage. It may lead to situations like data corruption			
	A brown-out protection circuit holds the processor/controller in reset state, when the			
	operating voltage falls below the threshold, until it rises above the threshold voltage			
	Certain processors/controllers support built in brown-out protection circuit which monitors			
	the supply voltage internally. If the processor/controller doesn't integrate a built-in brown-out			
	protection circuit, the same can be implemented using external passive circuits or supervisor ICs			
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	Reset pulse			
	Oz Active low			
	$\sim \sim $			
	>			
	GND			
	Agrap .			
		<u> </u>		



	Protection Systems			
	•Most of the modern operating systems are designed in such a way to support multiple users			
	with different levels of access permissions (e.g. Windows XP with user permissions like			
	• 'Administrator', 'Standard', 'Restricted', etc.). Protection deals with implementing the			
	security policies to restrict the access to both user and system resources by different			
	applications or processes or users.			
	•In multiuser supported operating systems, one user may not be allowed to view or modify the			
	whole/portions of another user's data or profile details.			
	•In addition, some application may not be granted with permission to make use of some of the			
	system resources.			
	•This kind of protection is provided by the protection services running within the kernel.			
	Interrupt Handler			
	•Kernel provides handler mechanism for all external/internal interrupts generated by the			
	system.			
	•These are some of the important services offered by the kernel of an operating system.			
	•It does not mean that a kernel contains no more than components/services explained above.			
	•Depending on the type of the operating system, a kernel, may contain lesser number of			
	components/services or more number of components/services.			
	•In addition to the components/services listed above, many operating systems offer a number			
	of add-on system components/services to the kernel.			
	•Network communication, network management, user-interface graphics, timer services			
	(delays, timeouts, etc.), error handler, database management, etc. are examples for such			
	components/services.			
	•Kernel exposes the interface to the various kernel applications/services, hosted by kernel, to			
	the user applications through a set of standard Application Programming Interfaces (APIs).			
	•User applications can avail these API calls to access the various kernel application/services.			
5	The Real-Time Kernel	10	CO5	L2
	•The kernel of a Real-Time Operating System is referred as RealTime kernel.			
	•In complement to the conventional OS kernel, the Real-Time kernel is highly			
	specialised and it contains only the minimal set of services required for running the			
	user applications/tasks.			
	The basic functions of a Real-Time kernel are listed below:			
	☐ Task/Process management			
	☐ Task/Process scheduling			
	☐ Task/Process synchronisation			
	☐ Error/Exception handling			
	☐ Memory management			
	☐ Interrupt handling			
	☐ Time management			
	Task/Process management			
	•Deals with setting up the memory space for the tasks, loading the task's code into the			
	memory space, allocating system resources, setting up a Task Control Block (TCB)			
	for the task and task/process termination/deletion.			
	•A Task Control Block (TCB) is used for holding the information corresponding to a			
	task.			
	•TCB usually contains the following set of information.			
	☐ Task ID: Task Identification Number			
	☐ Task State: The current state of the task (e.g. State = 'Ready' for a task which is			
	ready to execute)			
	☐ Task Type: Task typeIndicates what is the type for this task. The task can be a hard			
	real time or soft real time or background task.			
	☐ Task Priority: Task priority (e.g. Task priority = 1 for task with priority = 1)			
	Task Context Pointer: Context pointer-Pointer for context saving			
	Task Memory Pointers: Pointers to the code memory, data memory and stack			
	memory for the task			
	☐ Task System Resource Pointers: Pointers to system resources (semaphores, mutex,			
	etc.) used by the task			
	☐ Task Pointers: Pointers to other TCBs (TCBs for preceding, next and waiting tasks)			
	Other Parameters Other relevant taskparameters			
	•The parameters and implementation of the TCB is kernel dependent.			
	•The TCB parameters vary across different kernels, based on the task management			
	implementation. •Task management service utilises the TCB of a task in the following way.			
	•Task management service utilises the TCB of a task in the following way			

	•Creates a TCB for a task on creating a task			
	•Delete/remove the TCB of a task when the task is terminated or deleted			
	 •Reads the TCB to get the state of a task •Update the TCB with updated parameters on need basis (e.g. on a context switch) 			
	•Modify the TCB to change the priority of the task dynamically			
	Task/Process Scheduling			
	•Deals with sharing the PU among various tasks/processes.			
	•A kernel application called 'Scheduler' handles the task scheduling.			
	•Scheduler is nothing but an algorithm implementation, which performs the efficient			
	and optimal scheduling of tasks to provide a deterministic behaviour.			
	Task/Process Synchronisation			
	•Deals with synchronising the concurrent access of a resource, which is shared across			
	multiple tasks and the communication between various tasks.			
	Error/Exception Handling			
	•Deals with registering and handling the errors occurred/exceptions raised during the			
	execution of tasks.			
	•Insufficient memory, timeouts, deadlocks, deadline missing, bus error, divide by			
	zero, unknown instruction execution, etc. are examples of errors/exceptions.			
	Errors/Exceptions can happen at the kernel level services or at task level.			
	•Deadlock is an example for kernel level exception, whereas timeout is an example			
	for a task level exception.			
	•The OS kernel gives the information about the error in the form of a system call			
	(API). •GetLastError() API provided by Windows CE RTOS is an example for such a system			
	call.			
	•Watchdog timer is a mechanism for handling the timeouts for tasks.			
	•Certain tasks may involve the waiting of external events from devices.			
	•These tasks will wait infinitely when the external device is not responding and the			
	task will generate a hang-up behaviour.			
	•In order to avoid these types of scenarios, a proper timeout mechanism should be			
	implemented.			
	•A watch- dog is normally used in such situations.			
	•The watchdog will be loaded with the maximum expected wait time for the event and			
	if the event is not triggered within this wait time, the same is informed to the task and			
	the task is timed out.			
(•If the event happens before the timeout, the watchdog is resetted.		005	T 0
6	Mailbox Mailbox is an alternate form of 'Massaca groups' and it is used in contain Bool. Time	[5 5]	CO5	L2
	•Mailbox is an alternate form of 'Message queues' and it is used in certain Real- Time Operating Systems for IPC.	[3+3]		
	•Mailbox technique for IPC in RTOS is usually used for one way messaging.			
	•The task/thread which wants to send a message to other tasks/threads creates a mailbox for			
	posting the messages.			
	•The threads which are interested in receiving the messages posted to the mailbox by the			
	mailbox creator thread can subscribe to the mailbox.			
	•The thread which creates the mailbox is known as 'mailbox server' and the threads which			
	subscribe to the mailbox are known as 'mailbox clients'.			
	•The mailbox server posts messages to the mailbox and notifies it to the clients which are			
	subscribed to the mailbox.			
	•The clients read the message from the mailbox on receiving the notification.			
	•The mailbox creation, subscription, message reading and writing are achieved through OS			
	kernel provided API calls, Mailbox and message queues are same in functionality.			
	•The only difference is in the number of messages supported by them.			
	•Both of them are used for passing data in the form of message(s) from a task to another			
	task(s). Mailbox is used for exchanging a single message between two tasks or between an Interrupt Service Routine (ISR) and a task.			
	•Mailbox associates a pointer pointing to the mailbox and a wait list to hold the tasks			
	waiting for a message to appear in the mailbox.			
	•The implementation of mailbox is OS kernel dependent.			
	•The MicroC/OS-II implements mailbox as a mechanism for inter-task communication.			
	•Figure given below illustrates the mailbox based IPC technique			
	<u> </u>			



the respective processes. The result of the competition is 'deadlock'.

None of the competing process will be able to access the resources held by other processes since they are locked by the respective processes (If a mutual exclusion policy is implemented for shared resource access, the resource is locked by the process which is currently accessing it).

Mutual Exclusion: The criteria that only one process can hold a resource at a time. Meaning processes should access shared resources with mutual exclusion. Typical example is the accessing of display hardware in an embedded device.

Hold and Wait: The condition in which a process holds a shared resource by acquiring the lock control- ling the shared access and waiting for additional resources held by other processes.

No Resource Preemption: The criteria that operating system cannot take back a resource from a process which is currently holding it and the resource can only be released voluntarily by the process holding it.

Circular Wait:

A process is waiting for a resource which is currently held by another process which in turn is waiting for a resource held by the first process.

Deadlock Handling

The OS may adopt any of the following techniques to detect and prevent deadlock conditions.

Ignore Deadlocks:

Always assume that the system design is deadlock free. This is acceptable for the reason the cost of removing a deadlock is large compared to the chance of happening a deadlock.

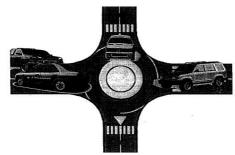
UNIX: is an example for an OS following this principle.

A life critical system cannot pretend that it is deadlock free for any reason.

Detect and Recover:

This approach suggests the detection of a deadlock situation and recovery from it. This one is similar to the deadlock condition that may arise at a traffic junction.

When the vehicles from different directions compete to cross the junction, deadlock (traffic jam) condition is resulted.deadlock (traffic jam) is happened at the junction, the only solution is to back up the vehicles from one direction and allow the vehicles from opposite direction to cross the junction. If the traffic is too high, lots of vehicles may have to be backed up to resolve the traffic jam. This technique is also known as **'back up cars' technique** (Fig. 10.26).



(Fig. 10.26) 'Back up cars' technique for deadlock recovery

Operating systems keep a resource graph in their memory. The resource graph is updated on each resource request and release. A deadlock condition can be detected by analysing the resource graph by graph analyser algorithms. Once a deadlock condition is detected, the system can terminate a process or preempt the resource to break the deadlocking cycle.

Avoid Deadlocks: Deadlock is avoided by the careful resource allocation techniques by the Operating System. It is similar to the traffic light mechanism at junctions to avoid the traffic jams.

Prevent Deadlocks: Prevent the deadlock condition by negating one of the four conditions favouring the deadlock situation.

Ensure that-a process does not hold any other resources when it requests a resource. This can be achieved by implementing the following set of rules/guidelines in allocating resources to pro- cesses.

- 1. A process must request all its required resource and the resources should be allocated before the process begins its execution.
- 2. Grant resource allocation requests from processes only if the process does not hold a resource currently.

Ensure that resource preemption (resource releasing) is possible at operating system level. This can be achieved by implementing the following set of rules/guidelines in resources allocation and releasing.

- 1. Release all the resources currently held by a process if a request made by the process for a new resource is not able to fulfil immediately.
- 2. Add the resources which are preempted (released) to a resource list describing the resources which the process requires to complete its execution.
- 3. Reschedule the process for execution only when the process gets its old resources and the new resource which is requested by the process. Imposing these criterions may introduce negative impacts like low resource utilisation and starvation of processes.

Livelock

- The Livelock condition is similar to the deadlock condition except that a process in livelock condition changes its state with time.
- While in deadlock a process enters in wait state for a resource and continues in that state forever without making any progress in the execution, in alivelock condition a process always does something but is unable' to make any progress in the execution completion.
- The livelock condition is better explained with the real world example, two people attempting to cross each other in a narrow corridor.
- Both the persons move towards each side of the corridor to allow the opposite person
 to cross. Since the corridor is narrow, none of them are able to cross each other. Here
 both of the persons perform some action but still they are unable to achieve their
 target, cross each other.

Starvation

- In the multitasking context, starvation is the condition in which a process does not get the resources required to continue its execution for a long time.
- As time progresses the process starves on resource.
- Starvation may arise due to various conditions like byproduct of preventive measures
 of deadlock, scheduling policies favouring high priority tasks and tasks with shortest
 execution time, etc.