



CBCS SCHEME

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Third Semester B.E. Degree Examination, June/July 2023

Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram and mathematical analysis explain fixed bias circuit. (06 Marks)
- b. With hysteresis characteristics explain the working of Inverting Schmitt trigger. (06 Marks)
- c. Explain current to voltage and voltage to current converter. (08 Marks)

OR

- 2 a. Discuss Regulated power supply parameters. (06 Marks)
- b. Explain the working of R-2R ladder D to A converter. (06 Marks)
- c. Explain successive approximation A to D converter. (08 Marks)

Module-2

- 3 a. Minimize the following function using K-map and implement it using basic gates.
 $f(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$ (06 Marks)
- b. Simplify the following function using Quine McClusky method.
 $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 10, 12, 13, 15)$ (08 Marks)
- c. Minimize the following function for POS using K-map and realize using basic gates
 $f(a, b, c, d) = \pi M(0, 1, 6, 8, 11, 12) + d(3, 7, 4, 15)$ (06 Marks)

OR

- 4 a. With an example explain Petrick's method. (06 Marks)
- b. Simplify the following function using Quine - McClusky method
 $f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (08 Marks)
- c. With the help of flow chart explain how to determine minimum sum of products using Karnaugh map. (06 Marks)

Module-3

- 5 a. Explain with neat diagram static 'O' hazard and how Static-O hazard can be detected and removed with example. (08 Marks)
- b. What is multiplexer, explain 8-to-1 multiplexer with the help of logic diagram and corresponding expression. (06 Marks)
- c. Explain with a neat diagram 3:8 decoder. (06 Marks)

OR

- 6 a. Implement the following function using PLA.
 $f_1(a, b, c) = \sum m(0, 4, 6, 7)$
 $f_2(a, b, c) = \sum m(4, 6)$ (06 Marks)
- b. Explain seven segment decoder and realize using PLA. (10 Marks)
- c. Explain simulation and testing of digital circuits. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Explain structure of VHDL program. Write VHDL code for 4 bit parallel adder using full adder as component. (08 Marks)
b. Explain the working of SR latch using NOR gates. (06 Marks)
c. Explain edge triggered D flip flop. (06 Marks)

OR

- 8 a. Explain J-K Master slave flip flop with suitable timing diagram. (10 Marks)
b. Derive the characteristics equations for D, T, SR and JK flip flops. (10 Marks)

Module-5

- 9 a. What is shift register? Explain the works of 8-bit SISO using SR flip flop with Timing diagram. (10 Marks)
b. With a block diagram explain the working of n bit parallel adder with accumulator. (10 Marks)

OR

- 10 a. Explain Three bit binary ripple counter with relevant waveforms and truth table. (10 Marks)
b. Design a random counter using T flip flop for the following sequence: (10 Marks)
000, 100, 111, 010, 011,
