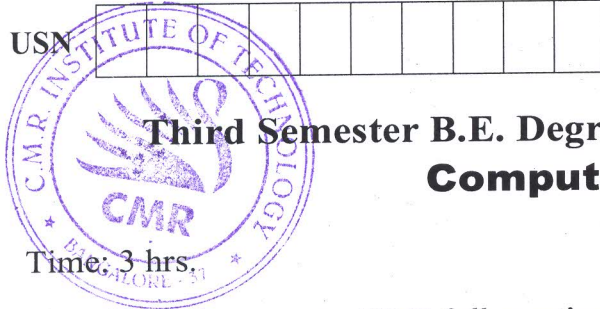


CBCS SCHEME

17CS34

USN



Third Semester B.E. Degree Examination, Dec.2023/Jan.2024 Computer Organization

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. What processor clock? Explain basic performance equation. (06 Marks)
- b. What is SPEC rating? Explain how the overall computer SPEC rating will be computed? (06 Marks)
- c. What are two ways that byte addresses can be assigned across words? Explain with neat diagram. (08 Marks)

OR

- 2 a. What is addressing mode? Explain with example, important addressing modes found in modern processors. (10 Marks)
- b. Using indirect addressing, write the assembly language code to perform the following:
The addresses of the memory locations containing the n-numbers represented as NUM1, NUM2,, NUM_n and Add instruction used to add each number to the register R₀ and then final SUM is placed in the memory location SUM. (10 Marks)

Module-2

- 3 a. With neat diagram, explain how a single interrupt request line may be used to serve n-devices. (06 Marks)
- b. What is vectored interrupts? Explain with neat diagram, implementation of interrupt priority using individual interrupt request and acknowledge lines. (06 Marks)
- c. What is exception? Describe the different kinds of exceptions. (08 Marks)

OR

- 4 a. What are Bus-Master and bus arbiter? Describe any one approaches of bus arbitration. (06 Marks)
- b. What is PCI bus? What are the important features of PCI bus? List and explain different data transfer signals on the PCI bus. (08 Marks)
- c. Describe the sequence of events that takes place, when the processor sends a command to the SCSI controller. (06 Marks)

Module-3

- 5 a. What is synchronous DRAM? With neat diagram, explain the structure of an SDRAM? Give the timing diagram for a typical burst read of length 4 in an SDRAM. (12 Marks)
- b. Design and explain the memory chip that can have an internal organization of a 1K × 1 memory chip. (08 Marks)

OR

- 6 a. With neat diagram, discuss the possible methods for specifying where memory blocks are placed in the cache memory. (10 Marks)
- b. What is memory interleaving? With neat diagram describe the two methods of memory interleaving. (06 Marks)
- c. Define the following terms:
- Average access time
 - The hit rate and miss rate
 - The miss penalty. (04 Marks)

Module-4

- 7 a. Design and implement 16-bit carry-look ahead adder using 4-bit adder blocks. (08 Marks)
- b. Give the block diagram showing the hardware arrangement for sequential multiplication, which performs multiplication by using a single n-bit adder. Hence compute the multiplication for the given multiplicand M : 1101 and multiplier Q : 1011. (12 Marks)

OR

- 8 a. Give circuit arrangement for binary division. Explain the restoring division algorithm for n-bit positive divisor M and n-bit positive dividend Q. (08 Marks)
- b. Perform the integer division using non-restoring-division algorithm given divisor M and n-bits and dividend n-bits. (06 Marks)
- c. Describe the IEEE standard floating point formats for, single precision and double precision. (06 Marks)

Module-5

- 9 a. With neat block diagram describe a three-bus structure used to connect the registers and the ALU of a processor. Give sequence of control instructions to perform Add R_4, R_5, R_6 . (10 Marks)
- b. What is micro programmed control? Describe the micro routine for the instruction Branch < 0 . (10 Marks)

OR

- 10 a. What is pipe lining? Explain the operation of four stage pipeline. (10 Marks)
- b. What is the purpose of control unit? With neat block diagram, explain the hardwired control unit in detail. (10 Marks)

CMRIT LIBRARY
BANGALORE - 560 037
