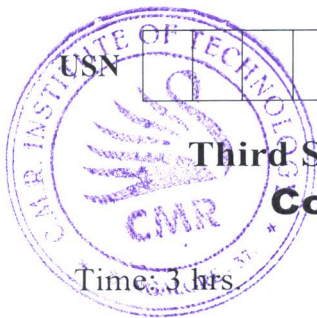


CBCS SCHEME

21CS34



Third Semester B.E. Degree Examination, Dec.2023/Jan.2024 Computer Organization and Architecture

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, explain basic operational concepts of a computer. (10 Marks)
- b. Define the basic performance equation. Summarize the measures to improve the performance. (05 Marks)
- c. Explain the overall SPEC rating for the computer in a programming suit. (05 Marks)

OR

- 2 a. What is addressing mode? Explain different types of addressing mode with examples. (10 Marks)
- b. Show the big and little endian assignments for the number 22354456. (05 Marks)
- c. Explain with basic types of the instruction formats to carry out $c \leftarrow [A] + [B]$. (05 Marks)

Module-2

- 3 a. Illustrate a program that reads one line from the keyboard, stores in memory buffer, and echoes it back to the display in an I/O interfaces. (05 Marks)
- b. Explain the following with respect to interrupts:
 - (i) Interrupt Nesting
 - (ii) Simultaneous requests(10 Marks)
- c. Define exception. Explain two kinds of exception. (05 Marks)

OR

- 4 a. With a neat diagram, explain the centralized arbitration scheme and distributed bus arbitration scheme. (10 Marks)
- b. With a neat timing diagram, illustrate the asynchronous bus data transfer during an input operation. Use Handshake scheme. (05 Marks)
- c. With neat diagram, explain how to connect keyboard to processor. (05 Marks)

Module-3

- 5 a. With a neat diagram, explain the organization of a $2M \times 32$ memory module using $512K \times 8$ static memory chips. (10 Marks)
- b. Explain different types of non volatile memories. (05 Marks)
- c. Explain with a neat block diagram of memory hierarchy in a contemporary computer system indicating variation of size, speed and cost per bit in the hierarchy. (05 Marks)

OR

- 6 a. Briefly explain any two mapping function used in cache memory. (10 Marks)
- b. With a diagram, explain how virtual memory address is translated. (05 Marks)
- c. Calculate the average access time experienced by a processor, if a cache hit rate is 0.88, miss penalty is 0.015 millisecond and cache access time is 10 micro seconds. (05 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, $42+8=50$, will be treated as malpractice.

Module-4

- 7 a. Convert the following numbers into signed 5 bit numbers and add them. Also, tell whether overflow has occurred or not. (i) 13, 5 (ii) -15, -7 (05 Marks)
- b. Explain with diagram the design and working of 16 bit carry look ahead adder built from 4-bit adders. (10 Marks)
- c. Solve the following using sequential circuit binary multiplier: (i) 11×13 (ii) 12×9 (05 Marks)

OR

- 8 a. With a neat diagram, explain single bus organization of computer. (10 Marks)
- b. List out the actions needed to execute the instruction Add (R3), R1. Write the sequence control steps for the execution of the same. (05 Marks)
- c. Explain with a neat diagram, micro-programmed control unit method for design of control unit. (05 Marks)

Module-5

- 9 a. Explain pipelining processing with example. (10 Marks)
- b. Explain processor with multiple functional units. (05 Marks)
- c. Explain arithmetic pipeline. (05 Marks)

OR

- 10 a. Explain four segment instruction pipeline. (10 Marks)
- b. Explain SIMD array processor. (05 Marks)
- c. Explain vector processing. (05 Marks)
