CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain construction and working principle of photo diode. **(08 Marks)**

b. Explain factors affecting the load voltage and performance parameters of a power supply. **(08 Marks)**

c. The base bias circuit is shown in Fig. Q1 (c) below for the value indicated, calculate I_B, I_C and V_{CE}. **(04 Marks)**

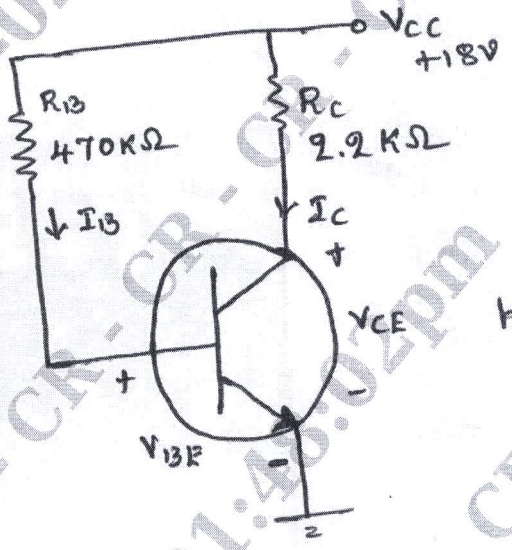

Fig. Q1 (c)

OR

2 a. With a neat diagram, explain R-2R ladder network DAC. Also mention its advantage over weighted resistive DAC. **(08 Marks)**

b. Design an astable multivibrator using 555 timer for a frequency of 2 kHz and a duty cycle of 75%. Assume $C_1 = 0.1\ \mu F$. **(08 Marks)**

c. Differentiate basic biasing techniques. **(04 Marks)**

Module-2

3 a. Determine the minimum sum of product expression and minimum product of sums expression for,

$f = \bar{b}\bar{c}\bar{d} + bcd + ac\bar{d} + \bar{a}\bar{b}c + \bar{a}\bar{b}\bar{c}d$

and also implement each derived expression using logic gates. **(10 Marks)**

b. Simplify the following using Quine McCluskey method, list primary implicants and identify essential prime implicants.

$f(A,B,C,D) = \sum m(3,4,5,7,10,12,14,15) + \sum d(2)$ **(10 Marks)**

OR

4 a. A switching circuit has two control inputs (C_1 and C_2), two data inputs (X_1 and X_2), and one output (Z). The circuit performs one of the logic operations AND, OR, EQU (Equivalence) or XOR (exclusive OR) on the two data inputs. The function performed depends on the control inputs.

C_1	C_2	Function performed by circuit
0	0	OR
0	1	XOR
1	0	AND
1	1	EQU

(i) Derive a truth table for Z.
(ii) Use a Karnaugh map to find a minimum AND-OR gate circuit to realize Z. **(10 Marks)**

b. For the following functions, find all the prime implicants and find all minimum sum-of-product solution. Using Quine Mc Cluskey method.
$f(a, b, c, d) = \sum m(0, 1, 3, 5, 6, 7, 8, 10, 14, 15)$ **(10 Marks)**

Module-3

5 a. Consider logic function : $F(A, B, C, D) = \sum m(0, 4, 5, 10, 11, 13, 14, 15)$
(i) Find two different minimum circuits which implement 'F' using AND-OR gates. Identify two hazards in each circuit. Then find an AND-OR circuit for 'F' which has no hazards.
(ii) Find the minimum OR-AND circuit for 'F' has two hazard. Identify it, and then find an OR-AND circuit for 'F' that has no hazards. **(10 Marks)**

b. Explain programmable logic devices. And implement full adder using PAL. **(10 Marks)**

OR

6 a. Illustrate 3 to 8 decoder with neat diagram. **(07 Marks)**

b. What is multiplexer? Explain working principle of 8-to-1 multiplexer with its logic diagram. **(07 Marks)**

c. Explain hazards in combinational logic circuits,
(i) Static-1 Hazard
(ii) Static-0 Hazard.
(iii) Dynamic Hazard. **(06 Marks)**

Module-4

7 a. Write a VHDL module for a 4-bit adder using structural description. **(08 Marks)**

b. Write VHDL code for,
(i) 2 : 1 MUX using VHDL statement and conditional assignment statement.
(ii) 4 : 1 MUX using VHDL statement and conditional assignment statement. **(08 Marks)**

c. Differentiate combinational and sequential circuits. **(04 Marks)**

OR

8 a. Assume that the inverter in the given circuit has a propagation delay of 5 ns and the AND gate has a propagation delay of 10 ns. Draw a timing diagram for the circuit showing x, y and z. Assume that x is initially 0, y is initially 1, after 10 ns, x becomes 1 for 80 ns and then x is 0 again.

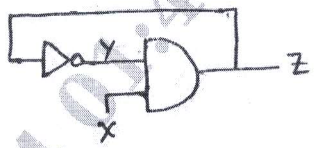

Fig. Q8 (a) **(08Marks)**

b. Convert the following by adding external gates,
   (i) A 'D' flipflops to a J-K flip-flop.
   (ii) A T flipflop to a D flip-flop. **(08 Marks)**

c. Differentiate Latches and flip-flops. **(04 Marks)**

Module-5

9 a. Explain with neat figure, how data can be transferred from the output of one of two registers into a third register using tri-state buffer. **(10 Marks)**

b. What is a shift register? Explain with neat diagram, a 4-bit right shift register. **(10 Marks)**

OR

10 a. Design a 3 bit synchronous binary counter using D-flip flops. **(10 Marks)**

b. Design a counter to generate sequence 0, 4, 7, 2, 3, 0 ….. using T flip flop. **(10 Marks)**

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