CBCS SCHEME

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18EE46

Fourth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Operational Amplifiers and Linear ICs

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define and explain the following terms:
(i) Input bias current (ii) Input offset current (iii) CMRR **(06 Marks)**

b. The circuit is to provide a gain of 10 at a peak frequency of 16 kHz. Determine the values of all components. Assume internal resistance T and the inductor be 30 Ω and C = 0.01 μF. [Refer Fig.Q1(b)]

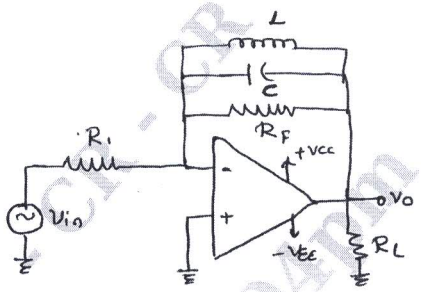

Fig.Q1(b) **(06 Marks)**

c. Explain the effect of feedback on input resistance R and output resistance for voltage shunt amplifier. **(08 Marks)**

OR

2 a. Explain the general stages of op-amps with a neat block diagram. **(08 Marks)**

b. What is an instrumentation amplifier? Obtain an expression for output voltage V_o in terms of change in resistance ΔR of an instrumentation amplifier using transducer bridge. **(12 Marks)**

Module-2

3 a. Using a 741 op-amp design the first order active low pass filter circuit to have a 1.0 kHz cut off frequency. **(06 Marks)**

b. Explain the following terms with respect to voltage regulator:
i) Line regulation ii) Load regulation iii) Ripple rejection **(06 Marks)**

c. With a neat diagram, explain the working of first order high pass filter and draw its typical frequency response curve. **(08 Marks)**

OR

4 a. Explain the working and design of an op-amp voltage follower regulator. **(08 Marks)**

b. The DC voltage source has $V_s = V_{cc} = 12V$, $V_o = 6.3V$, $R_1 = 270\ \Omega$, D_1 is a IN753 zener diode and $I_{L(max)} = 42$ mA. If the supply source resistance is 25 Ω, determine the line regulation, load regulation and ripple rejection for the circuit [IN753 $Z_z = 7\Omega$]. **(07 Marks)**

c. Briefly explain with the help of schematic diagram the working of LM317 IC regulator. **(05 Marks)**

Module-3

5 a. With a neat diagram explain the action of RC phase shift oscillator, write advantages and disadvantages of RC phase shift oscillator. **(10 Marks)**

b. Draw and explain triangular wave generator using square wave generator and integrator method. Draw the required waveforms. **(10 Marks)**

OR

6 a. With a neat diagram explain
(i) Comparator as zero crossing detector
(ii) Voltage to current converter with grounded load. **(10 Marks)**

b. With a neat circuit diagram explain non-inverting Schmitt trigger, if UPT is to be made 0V, explain the modification to be done in circuit, draw the relevant input / output waveform. **(10 Marks)**

Module-4

7 a. Explain the working principle of Linear Ramp Analog to Digital converter. **(06 Marks)**

b. Design a precision full wave rectifier circuit to produce a 2V peak output from a sine wave input with a 0.5V peak value and 1 MHz frequency. Use Bipolar op-amp with a supply voltage of ±15V. Choose adequate diode current as 500 μA. **(06 Marks)**

c. Explain the working of R-2R DAC with the help of neat diagram. **(08 Marks)**

OR

8 a. With a neat circuit diagram, explain the working of an non-saturation precision half wave rectifier and draw its input and output waveforms. **(07 Marks)**

b. With a neat diagram explain the working of op-amp sample and hold circuit. **(07 Marks)**

c. Explain the working of AD using successive approximation method. **(06 Marks)**

Module-5

9 a. Sketch the circuit diagram of an op-amp monostable multivibrator. Draw the circuit, waveforms and explain its operation. **(10 Marks)**

b. With a neat block diagram, explain phase locked loop in detail. **(10 Marks)**

OR

10 a. With a neat diagram explain the internal architecture of IC555 timer. **(08 Marks)**

b. Explain how X-OR gates can be used as phase detector in PLL. **(06 Marks)**

c. Write a note on PLL IC565. **(06 Marks)**

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