CBCS SCHEME

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17EE34

# Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
## Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

**Note:** *Answer any FIVE full questions, choosing ONE full question from each module.*



### Module-1

1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. **(10 Marks)**

b. What is the clamper? Explain the operation of positive clamper with reference :
i) Zero
ii) Positive ($V_R$)
iii) Negative ($-V_R$). **(10 Marks)**

**OR**

2 a. Design a voltage divider biasing circuit with a supply voltage of 10V and $V_{CE} = \frac{V_{CC}}{2}$. The load resistance is 2KΩ. Take β = 100. **(08 Marks)**

b. Derive the expression for stability factor for fixed bias circuit with respect to $I_{CO}$, $I_{BE}$ and β,. **(07 Marks)**

c. Explain how a transistor can be used as a switch. **(05 Marks)**

### Module-2

3 a. Draw the circuit of common emitter amplifier with voltage divider biasing. Derive the expression for current gain, voltage gain, input and output impedance using the h model. **(08 Marks)**

b. Derive equations for miller input capacitance and output capacitance. **(08 Marks)**

c. The h-parameter for the transistor are $h_{ie}$ = 1.1KΩ, $h_{fe}$ = 99, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe}$ = 25μA/v. Find h-parameters for CC configuration. **(04 Marks)**

**OR**

4 a. A voltage source of negligible internal resistance derives a common collector transistor amplifier. The load resistance is 2500Ω. The transistor h parameters are $h_{ic}$ = 1000Ω, $h_{rc}$ = 1, $h_{fc}$ = –50, $h_{oc}$ = 25μA/v. Compute $A_i$, $A_v$, $Z_i$ and $Z_0$. **(08 Marks)**

b. Starting from fundamentals, define h-parameters and obtain h-parameter equivalent circuit of CE configuration. **(08 Marks)**

c. Compare the characteristics of CB, CE and CC configuration. **(04 Marks)**

### Module-3

5 a. Drive expression for $Z_i$ and $A_i$ for a Darlington emitter follower circuit. **(10 Marks)**

b. An amplifier consists of 3 identical stages in cascade. If the bandwidth of the overall amplifier extends from 20Hz to 20KHz, calculate the bandwidth of the individual stage. **(06 Marks)**

c. List the advantages of negative feedback. **(04 Marks)**

**OR**

6 a. Draw the block diagram of voltage series feedback amplifier and find the effect of input and output impedance. **(10 Marks)**

b. Explain the need of a cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

c. An amplifier has a midband voltage gain of 1000 width $f_L$ = 50Hz and $f_H$ = 50KHz. If 5% feedback is applied, then calculate $f_L$ and $f_H$ with feedback. **(04 Marks)**

## Module-4

7 a. Explain the operation of class B push pull amplifier. Prove that the maximum efficiency of class B configuration is 78.5%. **(08 Marks)**

b. Explain the classification of power amplifier with neat circuit diagram and waveforms of collector current and collector voltage for each type of power amplifier. **(08 Marks)**

c. A crystal has the following parameters : L = 3H, $C_s$ = 0.05pF, R = 2KΩ, $C_m$ = 10pF. What are the series and parallel resonant frequencies of the crystal? **(04 Marks)**

**OR**

8 a. Derive an expression for frequency of oscillation of RC phase shift oscillator. **(10 Marks)**

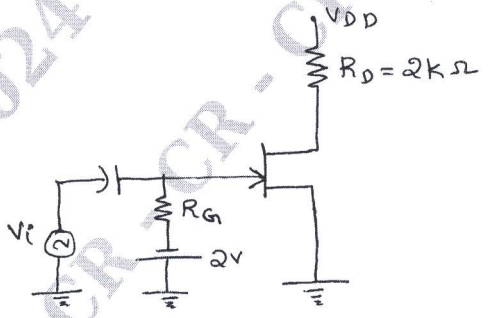
b. Explain the principle of operation of oscillator and the effect of loop gain ($A_\beta$) on the output of oscillator. **(06 Marks)**

c. The following distortion readings are available for a power amplifier :
$D_2$ = 0.1, $D_3$ = 0.02, $D_4$ = 0.03 with $I_1$ = 4A, $R_C$ = 8Ω.
Calculate :
i) Total harmonic distortion
ii) Fundamental power
iii) Total power. **(04 Marks)**

## Module-5

9 a. With a neat diagram, explain the construction and working and characteristics of n channel JFET. **(10 Marks)**

b. For the following circuit, find voltage gain and output impedance :
i) if $r_d$ = 20KΩ ii) $r_d$ = ∞. (Refer Fig.Q9(b))




$V_{DD}$ = 10V

$I_{DSS}$ = 10mA

$V_P$ = –4V

Fig.Q9(b) **(10 Marks)**



**OR**

10 a. Explain the construction, working and characteristics of n-channel enhancement type MOSFET. **(10 Marks)**

b. Draw the circuit of common source amplifier using JFET. With the help of small signal model derive an expression for input impedance, voltage gain and output impedance. **(10 Marks)**

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