CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Simplify using K map
   i) $f(a, b, c, d) = \Sigma m (0, 1, 4, 8, 9, 10) + d (7,11)$
   ii) $f(a, b, c, d) = \pi m (0, 1, 4, 10, 11, 14, 15)$ **(08 Marks)**

b. Convert the given function into corresponding canonical formula and decimal notation form
   i) $f(a, b, c) = ab + a\bar{c} + bc$
   ii) $f(a, b, c) = (a + b)(b + c)$ **(08 Marks)**

c. Define Canonical minterm formula and Canonical maxterm formula. **(04 Marks)**

OR

2 a. Find the minimal sum and minimal product for the given Boolean function
$f(a, b, c, d) = \Sigma m (2, 3, 4, 5, 13, 15) + d (8, 9, 10, 11)$ **(06 Marks)**

b. Simplify using K map
$f(a, b, c, d, e) = \Sigma m (0, 1, 4, 5, 7, 8, 9, 12, 13, 15, 21, 23, 29, 31)$ **(06 Marks)**

c. Simplify using Quine - Mc Cluskey method.
$f(a, b, c, d) = \Sigma m (0, 2, 8, 10, 12)$ **(08 Marks)**

Module-2

3 a. With a neat diagram, explain the operation of a look ahead carry generator. **(08 Marks)**

b. Implement the given function using
   i) 8 : 1 MUX with a, b, c as select lines
   ii) 4 : 1 MUX with a, b as select lines
$f(a, b, c, d) = \Sigma m (4, 5, 7, 8, 10, 12, 15)$ **(08 Marks)**

c. Design a 16:1 MUX using 4:1 MUX. **(04 Marks)**

OR

4 a. What is a magnitude comparator? Design a 2 bit magnitude comparator. **(08 Marks)**

b. Implement the multiple output function using 3:8 decoder with active low output lines
$F_1(a, b, c) = \Sigma m (1, 4, 5, 7)$
$F_2(a, b, c) = \pi m (2, 3, 6, 7)$ **(06 Marks)**

c. Design a logic circuit with inputs P, Q, R so that output is high wherever P = 0 or Q = R = 1. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain the working of a master slave JK flipflop along with waveforms. **(10 Marks)**

b. With a neat diagram, explain different modes of operation of universal shift register. **(10 Marks)**

OR

6 a. Give the logic diagram and counting sequence of ring counter and Johnson counter. **(06 Marks)**

b. Derive the characteristics equation of SR, JK, D and T flipflop. **(08 Marks)**

c. Design a mod 6 synchronous counter using T Flip Flop. **(06 Marks)**

Module-4

7 a. Compare Mealy and Moore synchronous sequential circuit with neat block diagram. **(08 Marks)**

b. Design a counter with the sequence 7, 4, 3, 1, 6, 0, 7 with JK flipflop **(12 Marks)**

OR

8 a. Analyze the given synchronous sequential circuit given below and draw the state table and state diagram.

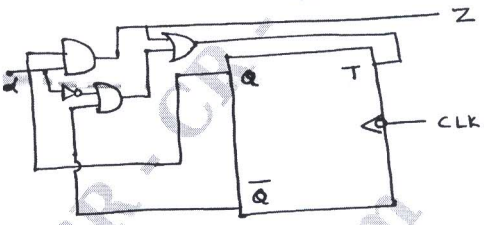

Fig Q8(a) **(10 Marks)**

b. Construct a sequential circuit with single input single output by obtaining the state and excitation table for the given diagram using JK Flipflap.

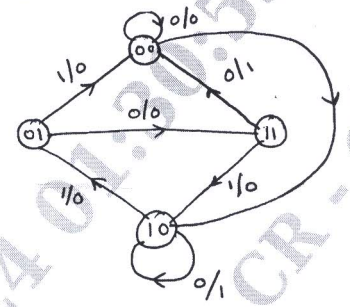

Fig Q8(b) **(10 Marks)**

Module-5

9 a. Explain the structure of VHDL module and verilog module with an example of half adder. **(10 Marks)**

b. Explain the shift operators of VHDL and verilog with an example. **(10 Marks)**

OR

10 a. Explain the data types available in VHDL. **(10 Marks)**

b. Explain the structure of behavioural description and data flow description with a suitable example. **(10 Marks)**

* * * * *