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Third Semester B.E. Degree Examination, Dec.2023/Jan.2024 Analog Electronic Circuits

Time: 3 hrs

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Draw the neat circuit diagram for negative clamper and explain with suitable waveforms. (06 Marks)
- b. For the transistor circuit shown in Fig. Q1 (b), determine R_B and R_C . Take $I_{C(sat)} = 12 \text{ mA}$, $\beta = 200$, $V_{CE(sat)} = 0 \text{ V}$. (06 Marks)

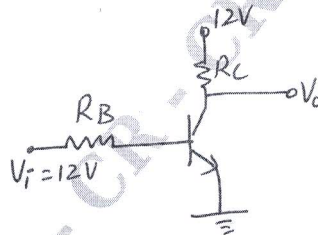


Fig. Q1 (b)

- c. Determine the Q-points (I_{CQ} , V_{CEQ}) for the circuit diagram shown in Fig. Q1 (c). Also find V_B , V_C , V_{BC} . (08 Marks)

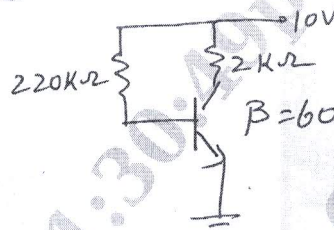


Fig. Q1 (c)

OR

- 2 a. Derive the expression for stability factor for Emitter Bias circuit with respect to I_{CO} and V_{BE} . (08 Marks)
- b. For the circuit shown in Fig. Q2 (b) with $\beta = 100$ and $I_C = 2 \text{ mA}$ for Si transistor. Calculate V_{CE} , R_E and stability factor $S(I_{CO})$. (08 Marks)

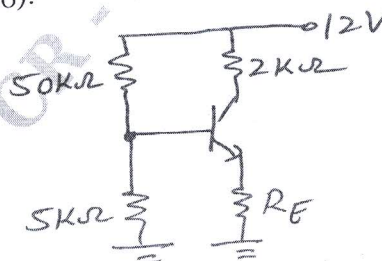


Fig. Q2 (b)

- c. Determine the stability factor $S(V_{BE})$ and change in I_C from 25°C to 100°C for transistor with $V_{BE}(25^\circ\text{C}) = 0.65 \text{ V}$ and $V_{BE}(100^\circ\text{C}) = 0.48 \text{ V}$ for fixed bias arrangement with $R_B = 270 \text{ k}\Omega$ and $\beta = 120$. (04 Marks)

Module-2

- 3 a. Derive the expression for Miller Input capacitance with suitable circuit diagram. (07 Marks)
 b. For the circuit shown in Fig. Q3 (b), draw neat simplified h-parameter model circuit and obtain the expression for current gain and voltage gain. (06 Marks)

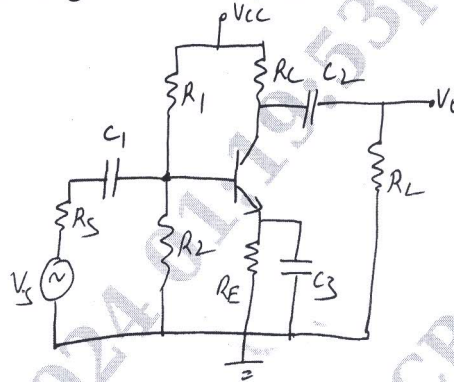


Fig. Q3 (b)

- c. For the amplifier shown in Fig. Q3 (b) with $h_{fe} = 50$, $h_{ie} = 1.1 \text{ k}\Omega$, $h_{oe} = 25 \text{ }\mu\text{A/V}$, $h_{re} = 2.5 \times 10^{-4}$, $R_1 = 50 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, $R_C = 2 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$, $R_S = 1 \text{ k}\Omega$. Calculate Input impedance, Output impedance, Current gain and Voltage gain. (07 Marks)

OR

- 4 a. Compare the relation between the parameters of simplified hybrid model and r_e model of the transistor in CE configuration with appropriate circuit diagram and expressions. (04 Marks)
 b. Obtain the expression for Input impedance, Output impedance and voltage gain of Emitter-follower configuration using AC equivalent circuit with r_e model. (08 Marks)
 c. For the Emitter-follower configuration with $V_{CC} = 12 \text{ V}$, $R_B = 220 \text{ k}\Omega$, $R_E = 3.3 \text{ k}\Omega$, $\beta = 100$ and $r_0 = \infty$. Calculate r_e , Z_i , Z_o and A_v . (08 Marks)

Module-3

- 5 a. For the cascaded arrangement shown in Fig. Q5 (a), determine the loaded gain for each stage, total gain for the system (A_v), total current gain and total gain (A_v), if the emitter-follower configuration were removed. (10 Marks)

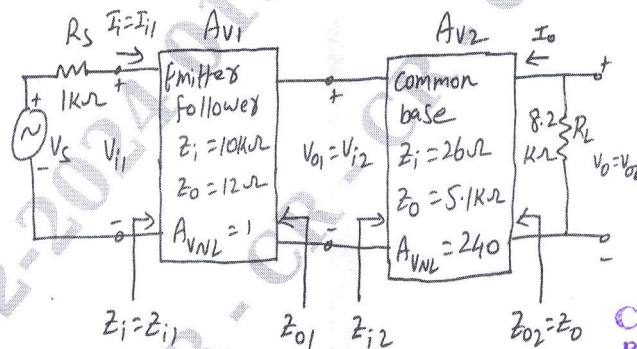


Fig. Q5 (a)

- b. For the Darlington emitter-follower with $V_{CC} = 18 \text{ V}$, $R_B = 3.3 \text{ M}\Omega$, $R_E = 390 \text{ }\Omega$, $r_i = 5 \text{ k}\Omega$, $\beta_D = 8000$, $V_{BE} = 1.6 \text{ V}$. Calculate the dc bias voltages (V_B , V_E , V_C), Currents (I_B , I_C), Input impedance, Output impedance, Voltage gain and Current gain. (10 Marks)

OR

- 6 a. Derive an expression for Input impedance of voltage series feedback and voltage shunt feedback amplifiers with suitable circuit connections. (10 Marks)
 b. Calculate the gain of a negative feedback amplifier having $A = -2000$, if feedback factor is 20%. (04 Marks)
 c. List the important characteristics and applications of Darlington Emitter follower. (06 Marks)

Module-4

- 7 a. For the circuit shown in Fig. Q7 (a), the dc base current is 5 mA and the ac input signal results in a peak base current swing of 4 mA. Assume Si transistor with $\beta = 30$. Determine ac power delivered to the load, dc power drawn by the circuit and conversion efficiency. (10 Marks)

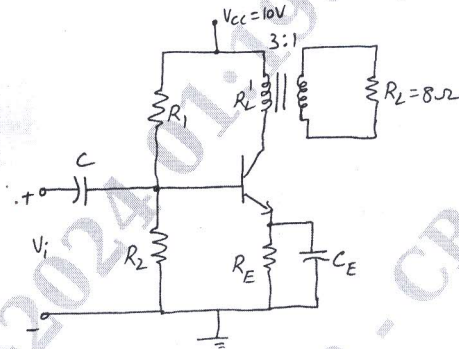


Fig. Q7 (a)

- b. A crystal has the following parameters : $L = 0.334$ H, $C = 0.065$ PF, $C_M = 1$ PF, $R = 5.5$ K Ω . Calculate the series resonant frequency and parallel resonant frequency. By what percent does the parallel-resonant frequency exceed the series resonant frequency? Also find the Q of the crystal. (10 Marks)

OR

- 8 a. Explain the operation of Wein bridge oscillator with appropriate circuit diagram and expressions. (07 Marks)
- b. For a Class B push-pull power amplifier with $V_{CC} = 25$ V driving an 8 Ω load, calculate maximum input power, maximum output power, maximum circuit efficiency, maximum collector dissipation and the input voltage at which maximum power dissipation occurs. (10 Marks)
- c. Write three merits of RC phase shift oscillator. (03 Marks)

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Module-5

- 9 a. For the FET amplifier shown in Fig. Q9 (a), calculate Z_i , Z_o and A_v . Also calculate Z_i , Z_o and A_v , neglecting the effect of r_d and compare the results. Take $I_{DSS} = 15$ mA, $V_P = -6$ V, $y_{OS} = 25\mu S$. (10 Marks)

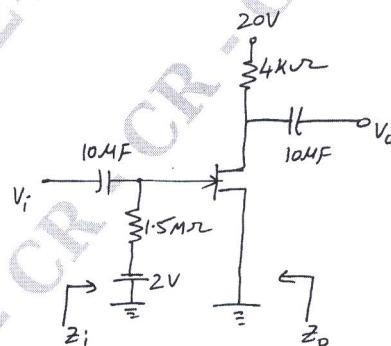


Fig. Q9 (a)

- b. Draw the circuit symbol and small signal ac model of D-MOSFET and E-MOSFET. Also derive the expression for transconductance g_m for both the MOSFET's. (10 Marks)

OR

- 10 a. For the circuit shown in Fig. Q10 (a), calculate Z_i , Z_o and A_v . Also find V_o if $V_i = 1 \text{ mV(rms)}$. (10 Marks)

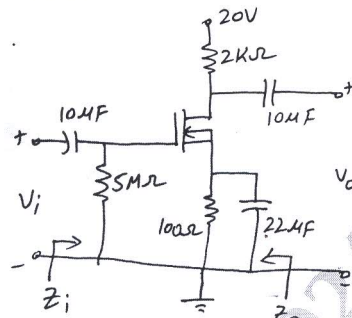


Fig. Q10 (a)

Take $I_{DSS} = 12 \text{ mA}$,
 $V_P = -3.5 \text{ V}$
 $V_{GSQ} = -0.75 \text{ V}$,
 $r_d = 50 \text{ K}\Omega$

- b. Explain the working and construction of JFET in detail and draw its transfer characteristics and drain characteristics. (10 Marks)

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