CBCS SCHEME

USN | | | | | | | | |

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital System Design

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a. What are prime implicants and essential prime implicants? Write them for the function $y = \sum m$ (0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15) and hence realize using NAND gates. **(06 Marks)**
   b. Simplify the following Boolean expression using K-map $f(A, B, C, D, E) = \sum m$ (0, 2, 4, 6, 8, 16, 18, 20, 22, 24, 26, 28, 30) + dc (3, 7, 11, 15, 19, 23, 27, 31). **(06 Marks)**
   c. Using Quine-Mc Cluskey method, obtain a minimal SOP expression of $f(a, b, c, d) = \sum m(1, 2, 6, 9, 10, 14) + dc(7, 8, 12)$. **(08 Marks)**

OR

2   a. Minimize the following expression in POS form using K-map:
      i) $f(A, B, C, D) = \pi M(0, 2, 3, 8, 9, 12, 13, 15)$
      ii) $f(A, B, C, D) = \pi M(0, 2, 4, 10, 11, 14, 15)$. **(06 Marks)**
   b. Design logic circuit that has 4 inputs, the output will be high when the majority of the inputs are high. Use K-map to simplify and realize using NAND gates. **(06 Marks)**
   c. Minimize the following expression using K-map and realize using NAND gates only:
      i) $f(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10) + dc(2, 11)$
      ii) $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 8, 9) + dc(10, 11, 12, 13, 14, 15)$. **(08 Marks)**

Module-2

3   a. What is a multiplexer? Design a 8:1 MUX and realize using NAND gates. **(06 Marks)**
   b. Realize using active high output 3 to 8 line decoder circuit and external gates
      i) $F_1(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 11, 15)$
      ii) $F_2(A, B, C, D) = \pi m(3, 6, 7, 14)$. **(08 Marks)**
   c. Draw the interface diagram of ten key interface to a digital system using decimal to BCD encoder. **(06 Marks)**

OR

4   a. Implement the Boolean expression $F(P, Q, R, S) = \sum m(0, 1, 3, 4, 8, 9, 15)$ using a 8:1 MUX choosing QRS as select lines. **(06 Marks)**
   b. Design 1 bit comparator using
      i) Basic gates   ii) Decoder of 2 to 4 line converter. **(06 Marks)**
   c. Write the sum and carryout equations of 4 bit look ahead parallel adder and hence realize the complete fast adder circuit. **(08 Marks)**

Module-3

5   a. What is race around condition in JK flip flops? Explain how to overcome from this problem. Explain with the help of waveform and logic diagram. **(06 Marks)**
   b. Explain the application of SR latch at a switch debouncer circuit. **(06 Marks)**
   c. Realize JK and T flip flop using NAND gates and hence derive the characteristic equation for the same. **(08 Marks)**

OR

6 a. With help of waveforms and output tabular column, explain master slave JK flip flop.
(08 Marks)

 b. Explain negative edge triggered D-flip flop and hence derive an expression for characteristic equation.
(06 Marks)

 c. Convert SR flip flop to a flip flop.
(06 Marks)

Module-4

7 a. Explain universal shift register using 4:1 multiplexers.
(08 Marks)

 b. With the help of wave form, logic diagram and output table, explain MOD5 ripple counter.
(06 Marks)

 c. Design a synchronous MOD 3 counter with the following sequence using clocked JK flip flop. Count sequence : 0, 1, 2, 0, 1, 2…..
(06 Marks)

OR

8 a. Explain MOD8 synchronous up down counter.
(06 Marks)

 b. With the help of waveforms, logic diagram and output table with respect to clock, explain MOD8 Johnson counter.
(08 Marks)

 c. Determine the frequency F_{max} for the synchronous MOD16 counter it delay t_{pd} for each flip flop is 50ηs and t_{pd} for each AND gate is 20ηs. Compare this with F_{max} for a MOD16 ripple counter. Determine the F_{max} for the MOD32 parallel counter. What has to be done to convert from MOD16 to MOD32 parallel counter?
(06 Marks)

Module-5

9 a. Explain Mealy and Moore model of a clocked synchronous sequence network.
(10 Marks)

 b. Analyze the synchronous circuit
  i) Write down the excitation and output function
  ii) Form the state table and diagram
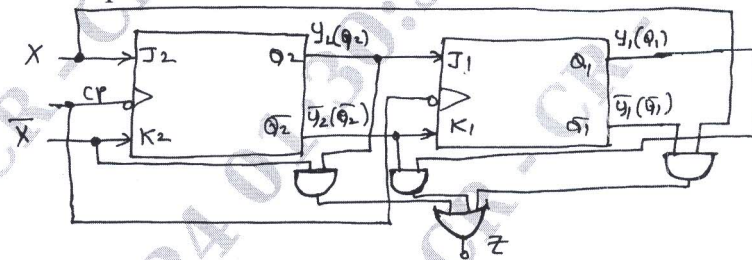 iii) Give a word description of the circuit operation.

Fig.Q.9(b)

(10 Marks)

OR

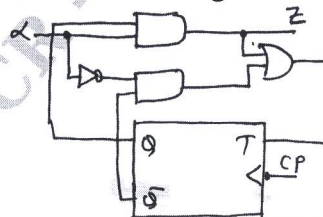10 a. Construct transition table, state table and state diagram for the given circuit.

Fig.Q.10(a)

(10 Marks)

 b. Design a synchronous counter using JK F/f to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2….. use state diagram and stable table. For the states 011 and 111, next state is 000.
(10 Marks)

* * * * *