CBCS SCHEME

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18EC56

Fifth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Discuss different levels of abstraction for describing a verilog HDL design, write the example in each case. **(10 Marks)**

b. Design a D-Flip Flop with synchronous reset, taking D-Flip Flop as an instance design a T-Flip flop also write a stimulus to verify the same. **(10 Marks)**

OR

2 a. Explain the typical design flow with verilog HDL for designing VLSI IC. **(08 Marks)**

b. What is a instance and instantiation? Explain with the help of an suitable example. **(06 Marks)**

c. Compare Top-down and Bottom-up design methodology. **(06 Marks)**

Module-2

3 a. Write a verilog code to implement the sequential circuit shown below Fig. Q3 (a), write the stimulus for the same. **(08 Marks)**

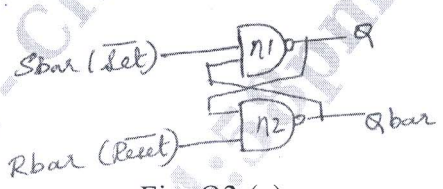

Fig. Q3 (a)

b. With a generated example, explain the component of verilog module. **(08 Marks)**

c. Explain : (i) 'define and (ii) 'include statements. **(04 Marks)**

OR

4 a. Explain the system tasks in verilog with example each:
(i) Nets (ii) Registers (iii) Array (iv) Parameter **(08 Marks)**

b. Define the following data type with an example. **(08 Marks)**

c. List in order the different signal strengths in verilog HDL. **(04 Marks)**

Module-3

5 a. Design a 4 : 1 Mux using primitives in verilog and write the logical diagram, Truth table, end logical expression for 4 : 1 mux. **(08 Marks)**

b. Discuss about (i) Rise (ii) Fall (iii) Turn-off delays. Also explain how their values are assumed when a (i) Single (ii) 2 (iii) 3 values are assigned to them in a statement. **(08 Marks)**

c. Design a gate level module for circuit shown below Q5 (c). **(04 Marks)**

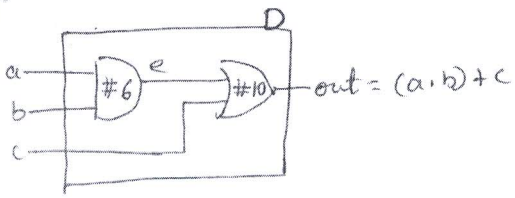

Fig. Q5 (c)

OR

6 a. Develop a gate level verilog code for a 4-bit ripple carry adder from 1-bit full adder. Write a stimulus to verify the design. **(08 Marks)**

b. With the help of a logic diagram and truth table explain bufif 0, bufif 1, notif 0, notif 1 gates. **(06 Marks)**

c. Write the truth table for all 1-bit operators. **(06 Marks)**

Module-4

7 a. With one suitable example, explain the non blocking statements. **(10 Marks)**

b. Explain : (i) Regular delay control (ii) Intra-assignment delay control
(iii) Zero delay control. **(06 Marks)**

c. Write a short note on automatic tasks and function. **(04 Marks)**

OR

8 a. Discuss with suitable examples, sequential and parallel blocks. **(08 Marks)**

b. Explain the following loops with suitable syntax and example :
(i) For loop (ii) Repeat loop (iii) While loop (iv) Forever loop **(08 Marks)**

c. List the differences between Tasks and Functions. **(04 Marks)**

Module-5

9 a. Write a short note on : (i) File output (ii) Initializing memory file. **(10 Marks)**

b. Explain the synthesis process if 4-bit magnitude comparator (which includes : Design specification, RTL description, Technology library, design constraints, logic synthesis) (Only stepwise description of the synthesis no diagram or program required) **(10 Marks)**

OR

10 a. Using the primitive gates, design a 1-bit full adder FA. Instantiate the full adder inside. Stimulus module. Force the sum output to a&b&cin for the time between 15 and 35 units. **(10 Marks)**

b. With a neat flow diagram, explain the process of computer aided logic synthesis. **(05 Marks)**

c. With the proper example describe and interpret the following verilog construct :
(i) always statement
(ii) function statement **(05 Marks)**

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