CBCS SCHEME

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15EC53

Fifth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the design flow of VLSI IC circuit steps with a neat flow chart. **(08 Marks)**
b. List the useful features of verilog HDL for hardware design. **(05 Marks)**
c. Explain the importance of HDL compared to traditional schematic based design. **(03Marks)**

OR

2 a. Explain TOP-down methodology applying to design of 4 bit Ripple carry counter. **(08 Marks)**
b. Explain the components of simulation. **(08 Marks)**

Module-2

3 a. With a neat block diagram, explain the components of verilog module. **(06 Marks)**
b. Explain the following data types with an example in verilog:
i) Nets ii) Register iii) Integers iv) Real v) Time Register. **(10 Marks)**

OR

4 a. Explain the port connection rules. **(06 Marks)**
b. Explain the two methods of connecting ports to external signals with an example. **(10 Marks)**

Module-3

5 a. Discuss on And/Or Gates with respect to logic symbols, gate instantiation and truth tables. **(08 Marks)**
b. Design AOI based 4:1 multiplexer, write verilog description for the same and its stimulus. **(08 Marks)**

OR

6 a. List the characteristics of continuous assignments. **(04 Marks)**
b. Write the verilog description of 4 bit full adder using dataflow operators and with carry look ahead mechanism. **(06 Marks)**
c. Discuss briefly available gate delays in verilog. **(06 Marks)**

Module-4

7 a. Describe multiway branching using case, case X, case Z with example. **(09 Marks)**
b. Write Behavioral modeling for 4 : 1 MUX using case statement. **(07 Marks)**

OR

8 a. Describe while, for, forever statements in verilog with syntax. **(09 Marks)**
b. Write behavioral modeling for 4 bit counter program in verilog. **(07 Marks)**

Module-5

9 a. Explain the synthesis process with a block diagram. **(08 Marks)**
b. Write a VHDL program for two 4-bit comparator using data flow description. **(08 Marks)**

OR

10 a. Explain the declaration of constant, variable and signal in VHDL with example. **(08 Marks)**
b. Write a VHDL program for half adder in behavioral description. **(08 Marks)**

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