CBCS SCHEME

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17EC53

Fifth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the process of VLSI IC designing using typical flow diagram. **(10 Marks)**
b. Explain briefly the importance of HDL. **(05 Marks)**
c. Explain component instance with an example. **(05 Marks)**

OR

2 a. Explain the design methodologies with an example for each. **(12 Marks)**
b. Explain the various abstraction levels used in verilog HDL. **(08 Marks)**

Module-2

3 a. Explain the following lexical conventions with an example for each.
i) Comments
ii) Operators
iii) Identifiers
iv) Keywords
v) Escaped identifiers. **(10 Marks)**
b. Explain the following data types with an example for each. **(10 Marks)**

OR

4 a. Explain the components of verilog module with neat block diagram and an example of SR latch. **(10 Marks)**
b. Explain the various port connection rules with a neat diagram and an example. **(06 Marks)**
c. Explain illegal port connection with an example. **(04 Marks)**

Module-3

5 a. Define the different types of gate delays and explain delay specifications in verilog with an example for each delay specification. **(10 Marks)**
b. A 2 input XOR gate can be built from my_and, my_or and my_not gates. Construct an XOR module in verilog that realizes the logic function, $Z = x\bar{y} + \bar{x}y$. Inputs are x and y, and z is the output. Write a stimulus module that exercise all four combination of x and y inputs. **(10 Marks)**

OR

6 a. Explain the equality operators with examples for all possible output conditions. **(10 Marks)**
b. Write a verilog description for 4:1 multiplexer using conditional operator in dataflow abstraction combinations of inputs. **(10 Marks)**

Module-4

7 a. Explain the structured procedure with suitable examples for each. **(10 Marks)**
b. Write a Verilog code for one bit comparator using if – else – if statement and a stimulus module that exercises all combinations of inputs. **(10 Marks)**

OR

8 a. Explain the following with suitable examples
i) Blocking assignments
ii) Non-blocking assignment (10 Marks)

b. Explain the following loops with examples :
i) While ii) For iii) Forever (10 Marks)

Module-5

9 a. Explain the synthesis, optimize and fitting the design process with a neat diagram. (10 Marks)

b. Explain the following with examples :
i) Constants
ii) Signals
iii) Variables (10 Marks)

OR

10 a. Explain the relationship between entity and architecture in VHDL with an example. (10 Marks)

b. What is an attribute? State the following attributes with an example for each :
i) 'left
ii) 'right
iii) 'high
iv) 'low
v) 'length
vi) 'range (10 Marks)

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