CBCS SCHEME

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15EC32

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive an expression for A_v, Z_i and Z_0 for CE–fixed bias using r_e-equivalent model. **(08 Marks)**

b. Define h-parameters and derive h-parameters model of CE-BJT. **(08Marks)**

OR

2 a. For the emitter-follower network of Fig.Q2(a). Determine : i) r_e ii) Z_i iii) Z_0 iv) A_V. **(08 Marks)**

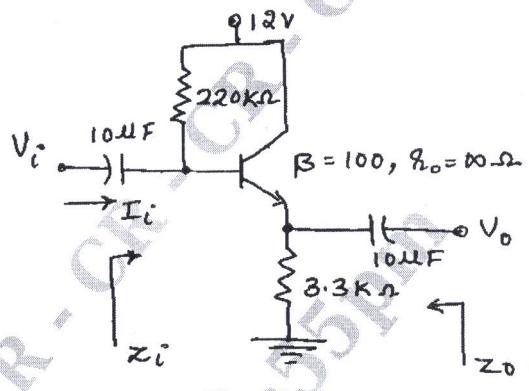

Fig.Q2(a)

b. With a neat circuit explain the high frequency transistor small-signal AC equivalent circuit. **(08 Marks)**

Module-2

3 a. With circuit diagram of JFET small signal model, determine g_m and r_d. **(08 Marks)**

b. For the JFET common-source amplifier using fixed-bias configuration. Derive expressions for Z_i , Z_0 and Av using AC equivalent circuit. **(08 Marks)**

OR

4 a. For the JFET common-gate configuration shown below, calculate Z_i, Z_0 and Av. **(08 Marks)**

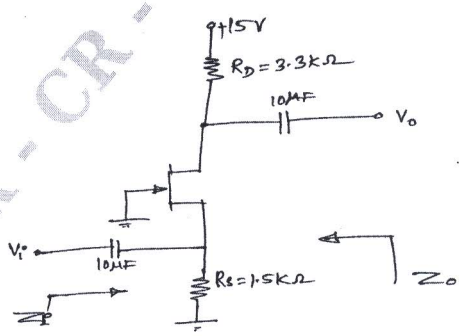

Fig.Q4(a)

b. With neat diagram, explain construction of n-channel JFET, and also draw its characteristics. **(08 Marks)**

Module-3

5 a. Prove that
Input capacitance is $C_{Mi} = (1 - A_v)C_f$ and
Output capacitance is $C_{MO} = \left(1 - \frac{1}{A_v}\right)C_f$ using miller effect. **(08 Marks)**

b. Describe the factors that affect the low frequency response of a BJT-CE amplifier. **(08 Marks)**

OR

6 a. Explain high frequency response of FET amplifier and derive expression for cut off frequencies, defined by input and output circuits (f_{Hi} and f_{Ho}). **(08 Marks)**

b. Determine the lower cut off frequency for the network shown in Fig. Q6 (b), using following parameters $g_m = 2$ ms, $r_d = \infty\Omega$, $I_{DSS} = 8$ mA, $V_P = -4V$, $V_{DD} = 20$ V. **(08 Marks)**

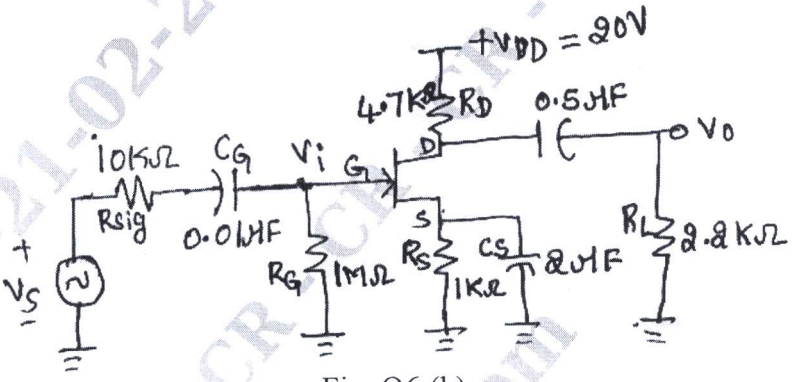

Fig. Q6 (b)

Module-4

7 a. Mention the types of feedback connections. Draw their block diagrams indicating input and output signal. **(08 Marks)**

b. With a neat circuit diagram, explain the working principle of FET phase–shift oscillator, with relevant equations. **(08 Marks)**

OR

8 a. What are the effects of negative feedback in an amplifier? Show how bandwidth of an amplifier increases with negative feedback. **(06 Marks)**

b. With a neat circuit and waveforms, explain the working operation of UJT relaxation oscillator. **(05 Marks)**

c. Determine the voltage gain, input and output impedance with feedback for voltage – series feedback having $A = -100$, $R_i = 10$ KΩ and $R_0 = 20$ kΩ for feedback factor $\beta = -0.1$. **(05 Marks)**

Module-5

9 a. Explain series – fed class – A power amplifier. Show that its maximum conversion efficiency is 25%. **(08 Marks)**

b. Explain with circuit diagram the operation of Class-B push-Pull amplifier using complementary–symmetry transistor pair. Also mention advantages and disadvantages of the circuit. **(08 Marks)**

OR

10 a. An ideal class –B push-pull power amplifier with input and output transformers has V_{CC} = 20V, $N_2 = 2N_1$ and $R_L = 20\Omega$. The transistors has $h_{fe} = 20$. Let the input be sinusoidal. For the maximum output signal at $V_{CE(P)} = V_{CC}$, determine :

i) The output signal power
ii) The collector dissipation in each transistor
iii) Conversion efficiency. **(08 Marks)**

b. The following distortion readings are available for a power amplifier, $D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$, with $I_1 = 3.3$A and $R_C = 4\Omega$.

i) Calculate the total harmonic distortion
ii) Determine the fundamental power component
iii) Calculate the total power. **(08 Marks)**

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