CBCS SCHEME

USN | | | | | | | | | | |

18EC35

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What are the basic functional units of a computer? Explain with neat sketch. **(10 Marks)**

b. Convert following Paris of numbers to 4-bit signed 2's compliment binary numbers, and add them. State whether an overflow occurs in each case.

i) +6 and +3 ii) +4 and –6 iii) –5 and –4 iv) – 8 and +1. **(08 Marks)**

c. State and explain basic performance equation. **(02 Marks)**

OR

2 a. With the aid of neat sketch explain basic operational concept of a computer. **(10 Marks)**

b. What do you mean by Big Endian and Little Endian? Explain with an example for each. **(06 Marks)**

c. What are conditional coders? Explain their significance. **(04 Marks)**

Module-2

3 a. Describe various modes of addressing with an example for each of them. **(10 Marks)**

b. Define an assembler directive. Explain any two assembler directives used in assembly language programming. **(06 Marks)**

c. Explain working of various shift instructions. **(04 Marks)**

OR

4 a. Explain the basic input/output operation performed by the processor with neat sketch. **(10 Marks)**

b. What is a stack? Explain how PUSH and POP operations are performed on a stack. **(10 Marks)**

Module-3

5 a. Describe any two methods of connecting multiple interrupting devices to the CPU. **(10 Marks)**

b. What is DMA? Explain DMA controller. **(10 Marks)**

OR

6 a. With neat diagram explain how simultaneous interrupt requests from multiple devices on single interrupting line is addressed using Daisy chain. **(10 Marks)**

b. Write a note on "Enabling and Disabling interrupts". **(10 Marks)**

Module-4

7 a. Draw the connection between memory and processor and explain how data transfer takes place between them. **(10 Marks)**

b. Draw and explain organization of SRAM and DRAM in detail. **(10 Marks)**

OR

8 a. What is a cache memory? Describe the elements of cache design. **(08 Marks)**

b. Draw and explain virtual memory organization. **(12 Marks)**

Module-5

9 a. With a neat sketch explain the single bus organization of processing unit. **(10 Marks)**

b. List and explain the control sequence for execution of the complete instruction "Add (R3), R1" for single bus architecture. **(10 Marks)**

OR

10 a. Explain in detail the organization of "hard wired control". **(10 Marks)**

b. Describe the organization of micro programmed control unit which allows conditional branching in the micro program. **(10 Marks)**

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