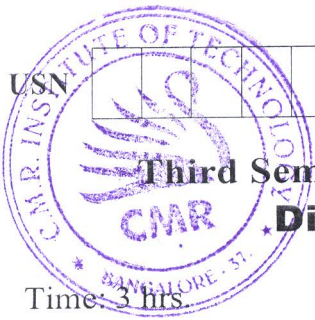


CBCS SCHEME

21EC32



Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital System Design using Verilog

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Define the following terms with an example
(i) Maxterms
(ii) Minterms
(iii) Combinational logic circuit (06 Marks)
- b. Place the following equations into the proper canonical form:
(i) $P = f(a, b, c) = ab' + ac' + bc$
(ii) $J = f(A, B, C, D) = (A + B' + C)(A' + D)$ (06 Marks)
- c. Design a combinational circuit to output the 2's complement of a 4-bit binary number. (08 Marks)

OR

- 2 a. Simplify the following Boolean function by using Q.M. method:
 $S = f(w, x, y, z) = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ (08 Marks)
- b. Obtain the simplified expression for the given four-variable equation using K-map and identify prime implicant and essential prime implicant.
 $K = f(w, x, y, z) = \sum(0, 1, 4, 5, 9, 11, 13, 15)$ (06 Marks)
- c. Explain briefly K-map, incompletely specified functions, essential prime implicants. (06 Marks)

Module-2

- 3 a. Implement $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ using:
i) 8 : 1 MUX with a, b, c as select lines
ii) 4 : 1 MUX with a, b as select lines (08 Marks)
- b. Explain the carry look ahead adder with necessary diagram and relevant expressions. (06 Marks)
- c. Design 4:2 line priority encoder which gives MSB the highest priority and LSB least priority. (06 Marks)

OR

- 4 a. Design 2-bit comparator using gates. (08 Marks)
- b. Explain the structure of programmable logic arrays with an example. (06 Marks)
- c. List the applications of decoder. Implement a full adder circuit using 3:8 decoder. (06 Marks)

Module-3

- 5 a. Explain Master-Slave SR flipflop with necessary truth table and timing waveforms. (06 Marks)
- b. Find characteristic equations for J-K and T flip-flops with the help of function tables. (06 Marks)
- c. Describe with neat diagrams the working and truth table of twisted ring counter and Mod-4 ring counter. (08 Marks)

OR

- 6 a. Explain serial-in serial out and serial-in parallel out unidirectional shift register with neat diagrams. (06 Marks)
b. Explain 4 bit synchronous binary counter with necessary timing waveforms. (06 Marks)
c. Design a synchronous Mod-6 counter using clocked JK flipflops. (08 Marks)

Module-4

- 7 a. Describe the structure of the verilog module with an example. (06 Marks)
b. Briefly explain the different data types in verilog. (08 Marks)
c. Write a verilog data flow description for full adder circuit. (06 Marks)

OR

- 8 a. Write a verilog code for 2:1 multiplexer with active low enable. (06 Marks)
b. Explain with an example how signal declaration and constant declaration is done in verilog. (06 Marks)
c. Discuss the shift operators and bitwise logical operators in verilog with examples. (08 Marks)

Module-5

- 9 a. Explain if-else structure and design a behavioral description of a D-latch using if statement. (06 Marks)
b. Realize 3:8 decoder using verilog behavioral description. (06 Marks)
c. Write a verilog description of a 4×4 bit Booth algorithm. (08 Marks)

OR

- 10 a. Write a structural description of a Half adder by describing the built in gates in verilog. (06 Marks)
b. Write a verilog structural description of ripple carry adder. (06 Marks)
c. Realize binary up/down counter using verilog behavioral description. (08 Marks)

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