CBCS SCHEME

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat diagram, explain basic operational concept of computer.	10	L1	CO1
	b.	Explain following with an example : i) Three address instruction ii) Two-address instruction iii) One-address instruction	06	L1	CO1
	c.	Explain Big Endian and Little Endian with neat diagram.	04	L1	CO1
		OR			
Q.2	a.	Discuss IEEE standard for single precision and double precision floating point numbers with example.	08	L1	CO1
	b.	What is system software? List functions of system software and explain how the processor is shared between user program and os routine.	08	L1	CO1
	c.	Explain computer basic performance equation.	04	L1	CO1
		Module – 2			
Q.3	a.	What is an addressing mode? Explain any five types of addressing modes with example.	10	L1	CO2
	b.	Write a program to add 'n' number using indirect addressing mode.	05	L2	CO2
	c.	Explain stack operations.	05	L2	CO2
		OR			
Q.4	a.	What are assembler directives? Explain various assembler directives used in assembly language program.	08	L2	CO2
	b.	Explain subroutine linkage with an example using linkage register.	06	L2	CO2
	c.	Explain the shift and rotate operations with example.	06	L2	CO2
		Module – 3			
Q.5	a.	Showing register configuration in I/O Interface, Explain program controlled input/output with program.	08	L2	CO2
	b.	Explain the registers involved in DMA interface.	06	L2	CO2
	c.	What is an interrupt? Explain interrupt hardware.	06	L2	CO2
		OR			
Q.6	a.	Explain the following method of handling interrupts from multiple devices. i) Daisy chain method ii) Priority structure	08	L2	CO3
	b.	What is Bus arbitration? Explain centralized bus arbitration mechanism with a neat diagram.	08	L2	CO3
	c.	Explain the concept of vectored interrupt.	04	L2	CO3
		Module – 4			
Q.7	a.	Explain internal organization of 16×8 memory chip.	08	L2	CO4
	b.	With a neat diagram, explain working principle of magnetic disk.	06	L2	CO4
	c.	With a neat diagram, explain virtual memory organization.	06	L2	CO2
		OR			
Q.8	a.	Explain the internal organization of 2M×8 DRAM chip with neat diagram.	08	L2	CO3
	b.	Explain a static RAM cell with a neat diagram.	06	L2	CO3
	c.	Discuss the concept of cache memory.	06	L2	CO3

Module – 5					
Q.9	a.	Explain with neat diagram, Single Bus organization of data path inside a processor.	08	L2	CO4
	b.	Discuss the control sequence for execution of instruction ADD (R3), R1.	06	L2	CO4
	c.	Describe the organization of hardwired control unit.	06	L2	CO4
OR					
Q.10	a.	Explain multiple bus/three bus organization with a neat diagram.	10	L2	CO5
	b.	What is microprogrammed control? Explain its basic organization with suitable diagram and example.	10	L2	CO5

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