CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. For a common Emitter with voltage divider bias, derive the expression fro voltage gain, input impedance and output impedance sign re model. **(10 Marks)**

b. For the networks shown in Fig.Q1(b).
   i) Determine
   ii) Find Z_i(with $r_0 = \infty$)
   iii) Calculate Z_0(with $r_0 = \infty$)
   iv) Determine A_V(with $r_0 = \infty$)

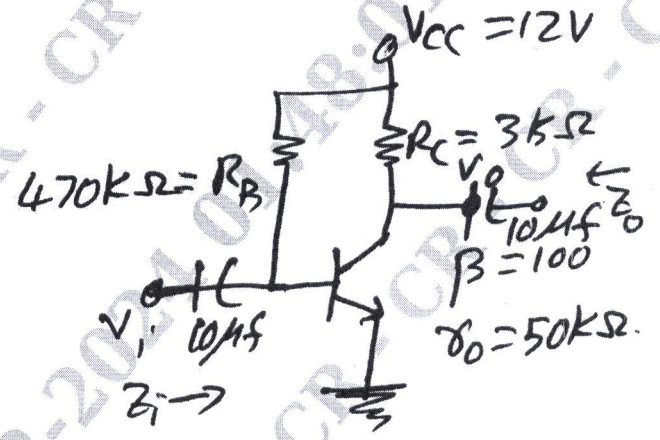

Fig.Q1(b) **(10 Marks)**

OR

2 a. Draw the complete hybrid equivalent (h-parameters model) circuit of two part networks for BJT and obtain equation for voltage gain and current gain. **(10 Marks)**

b. Draw circuit of Hybrid π-model of transistor and mention various parameters. **(10 Marks)**

Module-2

3 a. Explain construction and characteristics of n-channel JFET. **(08 Marks)**

b. Explain transfer characteristics of FET and mention the required equation. **(08 Marks)**

c. Mention differences between depletion type and enhancement type MOSFET. **(04 Marks)**

OR

4 a. Draw the circuit of common source voltage divider using JFET and derive the expression for Z_i, Z_0 and A_v. **(10 Marks)**

b. The self-bias configuration has operating point at $V_{GS} = -2.6V$, $I_{Dn} = 2.6mA$. The circuit is a shown in Fig.Q4(b).
Determine : i) g_m ii) r_d iii) Z_i iv) Z_0 v) A_V without r_d.

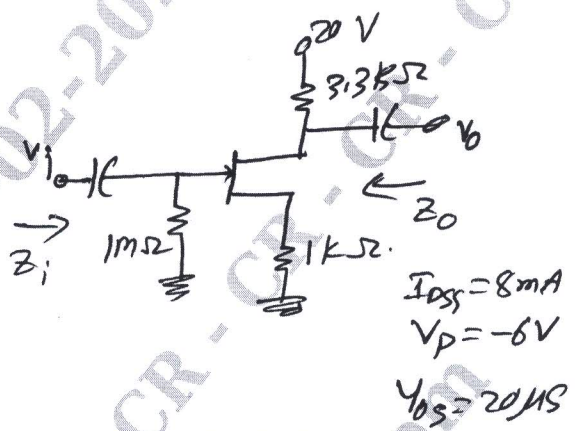

Fig.Q4(b) **(10 Marks)**

Module-3

5 a. Derive expression for lower cut-off frequency w.r.t C_g and mention the effect of C_C and C_E frequency. **(08 Marks)**

b. For FET amplifier circuit determine lower cut off frequency and sketch frequency response curve using the following parameters :
$C_Q = 0.01\mu f$, $C_C = 0.5\mu f$, $C_S = 2\ \mu f$, $R_{Sig} = 10K\Omega$,
$R_G = 1m\Omega$, $R_D = 4.7K\Omega$, $R_S = 1\ K\Omega$, $R_L = 2.2K\Omega$,
$I_{DSS} = 8mA$, $V_P = -4V$, $r_d = \infty\Omega$, $V_{DD} = 20V$. **(12 Marks)**

OR

6 a. Draw high frequency ac equivalent circuit of FET amplifier and obtain higher cut off frequency for i/p and o/p. **(12 Marks)**

b. With the help of suitable equations and neat diagram, explain the multistage frequency effect. **(08 Marks)**

Module-4

7 a. Draw the block diagram of voltage series feedback amplifier and derive the expression for gain with feedback, i/p and o/p impedances. **(10 Marks)**

b. Determine the voltage gain, i/p and o/p impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10K\Omega$, $R_0 = 20K\Omega$, for feedback factor of $B = -0.1$. **(06 Marks)**

c. State the merits of –ve feed back in amplifier. **(04 Marks)**

OR

8 a. Draw the circuit of phase shift oscillator using JFET and explain its operation. Also mention the equation of for frequency of oscillations. **(10 Marks)**

b. Draw the circuit of Wien Bridge oscillator and derive the expression for frequency of oscillation. Also explain the circuit connection and working. **(10 Marks)**

Module-5

9 a. Draw the circuit of series fed class-A amplifier and derive the expression for maximum efficiency with operation. **(10 Marks)**

b. Define harmonic distortion and calculate the harmonic distortion components for an o/p signal having the fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic of 0.1V and fourth harmonic amplitude of 0.05V, also find total harmonic distortion. **(10 Marks)**

OR

10 a. With the help of a block diagram, explain short voltage regulation and also explain how the same can be implemented using BJT. **(12 Marks)**

b. Calculate the output voltage and the zener current in the regulator circuit. Refer Fig.Q10(b).

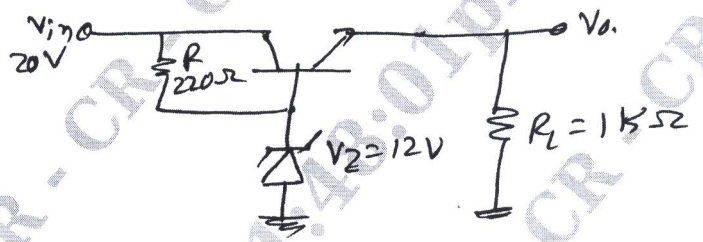

Fig.Q10(b) **(08 Marks)**

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