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CMR INSTITUTE OF TECHNOLOGY

Internal Assesment Test – I									
Sub:	**VLSI DESIGN**							**Code:**	**18EC72**
Date:	**30.10.2023**	**Duration:**	**90 mins**	**Max Marks:**	**50**	**Sem**	**VII**	**Branch**	**ECE-A,B,C,D**

Answer Any Five Questions

	Questions	Marks	OBE	
			CO	RBT
1.	Explain the operation of an n-channel enhancement mode MOSFET with neat diagrams.	[10]	CO1	L1
2.	Derive the expression for Drain to source current for an n-channel MOSFET in all three regions.	[10]	CO1	L2
3.	Describe in detail about any five non-ideal I-V characteristics of MOS transistor.	[10]	CO1	L1

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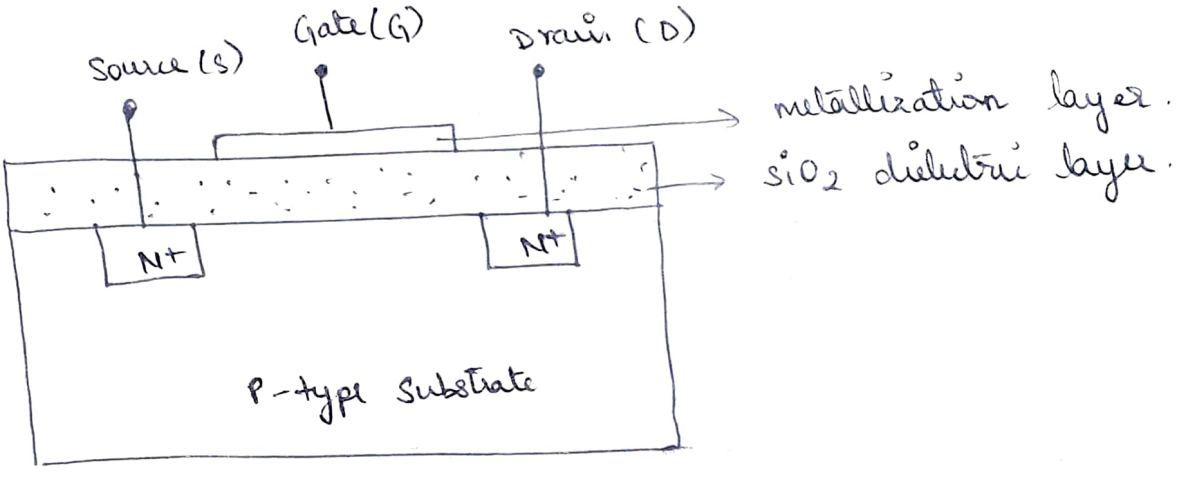
4.	Realize the following logic expression using CMOS: a) $Y = \overline{(A.B) + (C.D)}$ b) $Y = \overline{A + BC}$	[10]	CO1	L2
5.	Illustrate with neat sketch, explain the DC transfer characteristics of CMOS inverter.	[10]	CO1	L2
6.	With necessary circuit diagram, explain the operation of transmission gate. Also realize a 4:1 multiplexer using transmission gate.	[10]	CO1	L3

CI **CCI** **HOD**

INTERNAL ASSESSMENT - 01

Q1) Basic structure of n-channel enhancement mode MOSFET is shown below.



⇒ When the gate voltage is zero ($V_g = 0$) and no positive voltage is applied ~~across~~ between the source and drain (V_{ds}), the PN-junction is reverse-biased.

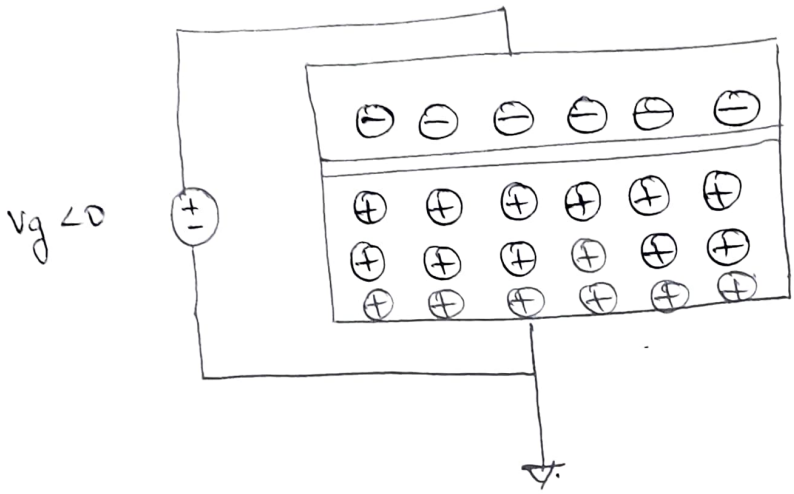
⇒ Since there is no current flow across the substrate and region below the gate, MOSFET is in OFF condition.

⇒ When a positive voltage is applied to the gate ie when the gate to source voltage increases, it induces an electric field E across the substrate which attracts electrons and repels holes.

⇒ At this condition, when the gate voltage is increased further, the gate of p-type changes to n-type.

⇒ Based on applied voltage, there are 3 modes of operation.

(i) Accumulation Mode:



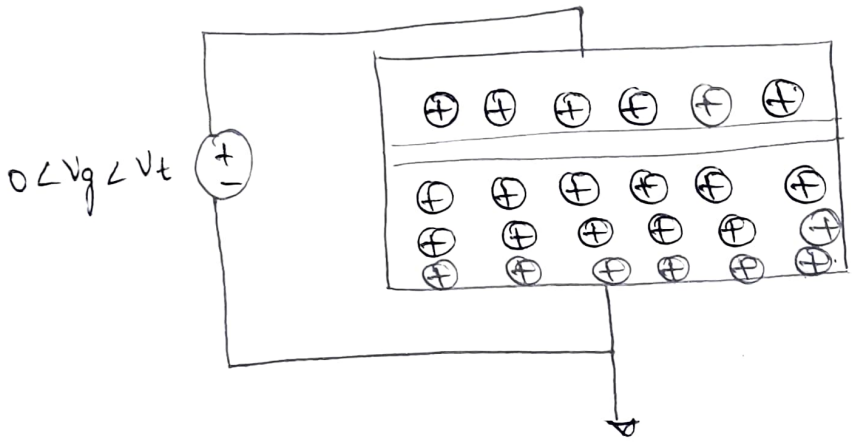
⇒ When the gate voltage is equal to 0 ($V_g = 0$) or voltage less than 0 is applied to the gate (-ve voltage), electron get accumulated at the region below the gate.

⇒ This mode is known as accumulation mode.

⇒ There is no conduction between the drain & source.

⇒ The device is in OFF condition.

(ii) Depletion mode.



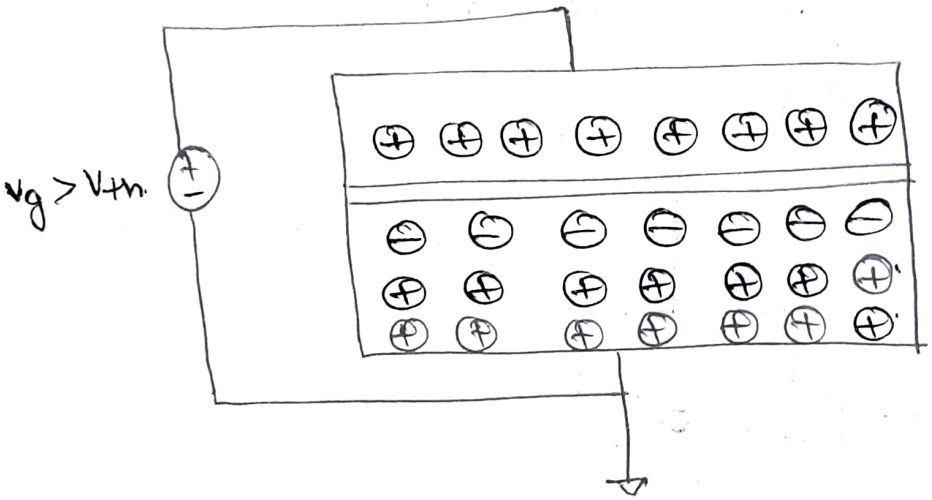
⇒ When voltage greater than 0 but less than threshold voltage is applied to the gate, it is known as depletion mode.

→ The electrons get attracted towards the gate and holes are repelled towards the region under gate.

→ This creates a depletion layer in the region below the gate and hence is known as depletion mode.

(iii) Inversion Mode.

Condition



Cut off / Linear / Sat

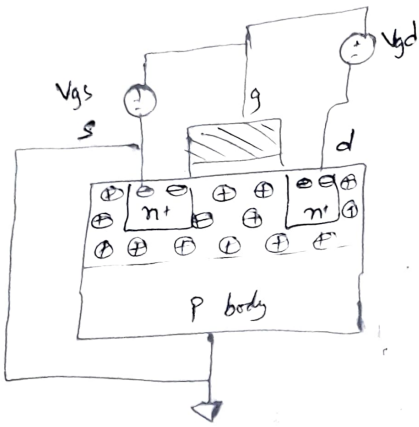
→ When the positive voltage is increased further i.e when the gate voltage is raised above threshold voltage, the electrons are attracted towards the substrate.

→ The holes are repelled towards the gate.

→ At this stage, on increasing the voltage p-type changes to n-type.

→ Conduction takes place in this mode.

→ Since electrons are attracted towards substrate & holes are repelled towards gate, an inversion layer is created.



→ $V_{gs} < V_t$

→ Transistor is in off state.

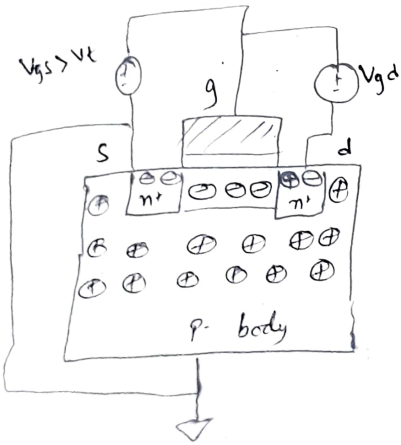
→ The junction between drain and source is reversed biased thus no current flows

→ $I_{ds} = 0$.

→ Also here is no channel formed.

→ Source is grounded.

→ It is called cut off region.



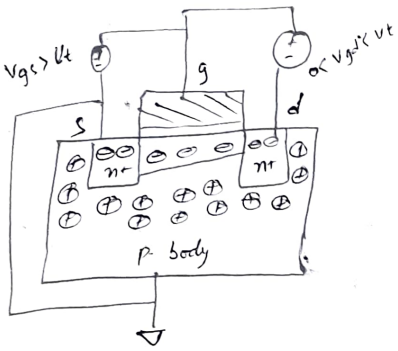
→ $V_{gs} > V_t$

→ $V_{gs} = V_{gd}$

→ The channel layer is formed b/w drain and source called inversion layer below the gate.

→ $V_{ds} = 0$.

iii) Linear Region.



→ $V_{gs} > V_t$

→ $V_{ds} = V_{gs} - V_{gd}$

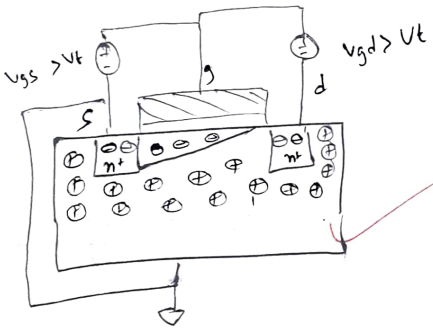
→ As $V_{ds} = 0$

$V_{gs} = V_{gd}$

→ The E-field push I_{ds} from drain to source.

→ This form a channel b/w source and drain called linear region.

iv) Saturation Region



→ $V_{gs} > V_t$

→ $V_{gd} > V_t$ (Saturate).

→ When $V_{out} > V_{gs} - V_t$ it forms saturation region, where the

→ layer gets pinched off towards the source.

→ Some of positive drop voltage is still present that cause e^- to flow.

Ans2.) In cut off region $V_{gs} < V_t$

There is no current flowing $\therefore$ $\boxed{I_{ds} = 0.}$ (cut off)

$Q = CV$ - (1)

$C = C_g = C_{ox} WL$ - (2) (Total capacitance) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$V = V_g - V_t$ - (3)

$V_g = \frac{V_{gs} + V_{gd}}{2}$ - (4)

$V_{ds} = V_{gs} - V_{gd}$ - (5)

$\therefore V_{gd} = V_{gs} - V_{ds}$ - (6)

putting (6) in (4)

$V_g = \frac{2V_{gs} - V_{ds}}{2} \Rightarrow V_g = V_{gs} - \frac{V_{ds}}{2}$ - (7)

Also $V = V_{gs} - \frac{V_{ds}}{2} - V_t$ - (8)

$V = \mu E$ (charge velocity) $t = \frac{L}{V} = \frac{L}{\mu E}$

$E = \frac{V_{ds}}{L}$

$I = \frac{Q}{t}$

$I_{ds} = \frac{C_g V}{t}$

$$I_{ds} = \frac{C_{ox} W \mathcal{E} \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right)}{\frac{\mathcal{E}}{\mu \mathcal{E}}}$$

$$= C_{ox} W \mu \mathcal{E} \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right)$$

$$= C_{ox} W \mu \frac{V_{ds}}{L} \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right) \quad \left[\because \mathcal{E} = \frac{V_{ds}}{L}\right]$$

$$\boxed{I_{ds} = C_{ox} W \mu \frac{V_{ds}}{L} \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right)} \rightarrow \text{Linear Region.}$$

For saturation region $\underline{V_{ds} = V_{gs} - V_t}$

$$\therefore I_{ds\,sat} = \beta V_{ds} \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right)$$

$$= \beta (V_{gs} - V_t) \left((V_{gs} - V_t) - \left(\frac{V_{gs} - V_t}{2}\right)\right)$$

$$\boxed{I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2} \rightarrow \text{Saturation region.}$$

$$\beta = \frac{C_{ox} W \mu}{L}$$

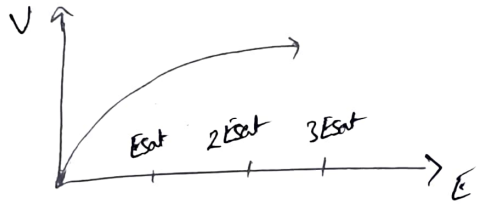
10

i) Charge mobility

$$V = \mu \vec{E}$$

→ μ is a constant term.

→ If $\vec{E}$ increases, then μ also increased which in turn increases the electron mobility that is 'V'. at $\vec{E}$ sat.



→ If V is not saturated

$$I_{ds} = \frac{\mu C_{ox} W L}{L} (V_{gs} - V_t)^2$$

→ If 'V' is saturated

$$I_{ds} = \mu C_{ox} W (V_{gs} - V_t) V_{ds}$$

→ From above eqn it can be seen that if V is saturated it is quadratically dependent and for saturation it is linearly dependent.

v) Body Effect

→ When potential between body and source is reduced is also affect the V_t.

→ Thus when V_t is also reduced it is called body effect.

→ Transistor has 4th implicit terminal called body.

$$V_t = V_{to} + \gamma \left(\sqrt{\phi_s - V_{SB}} - \sqrt{\phi_s} \right)$$

→ This equation gives the V_t dependence on γ

γ → Body pot. Coefficient

V_{to} : pot when V_t is at Saturation

ϕ_s : pot when body saturation.

vi) Junction Leakage

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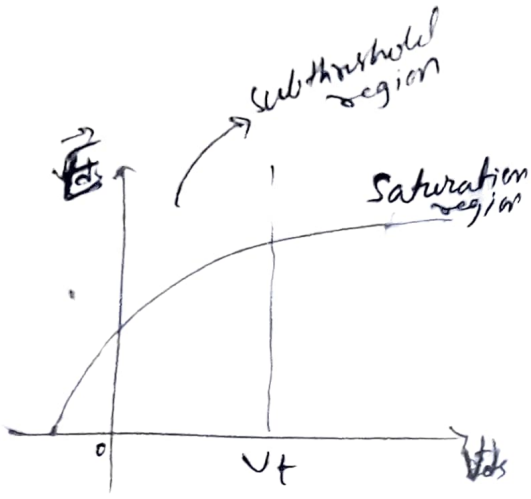
→ It is the leakage current when there is saturation.

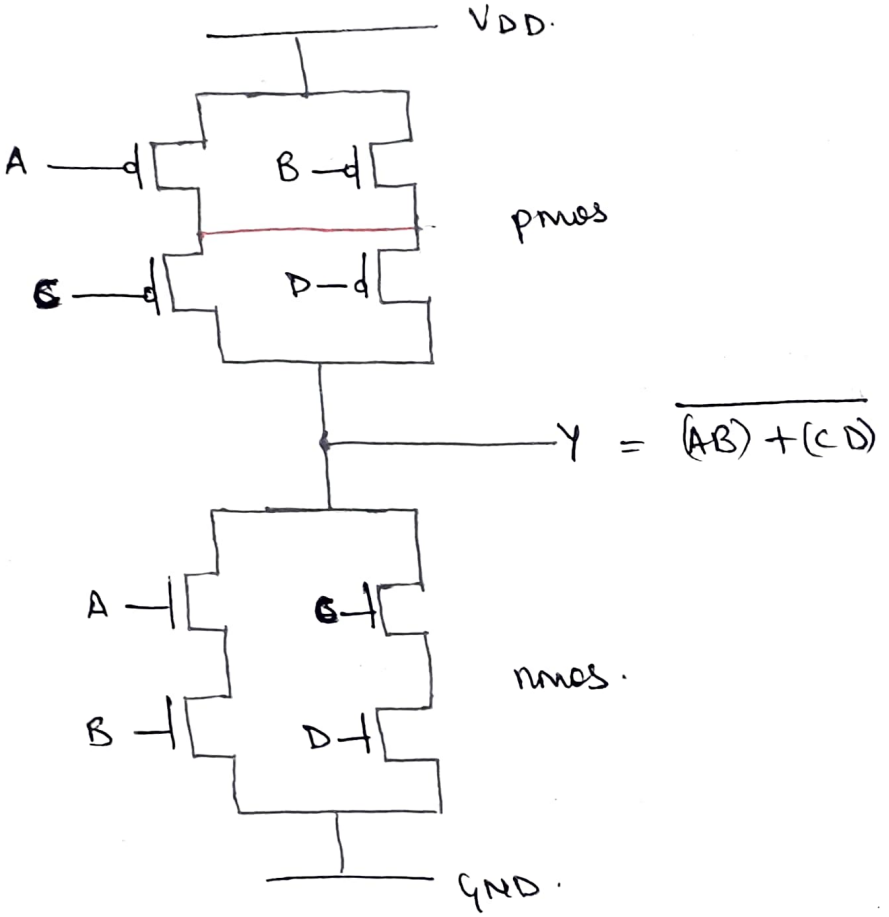
vii) Sub-threshold region



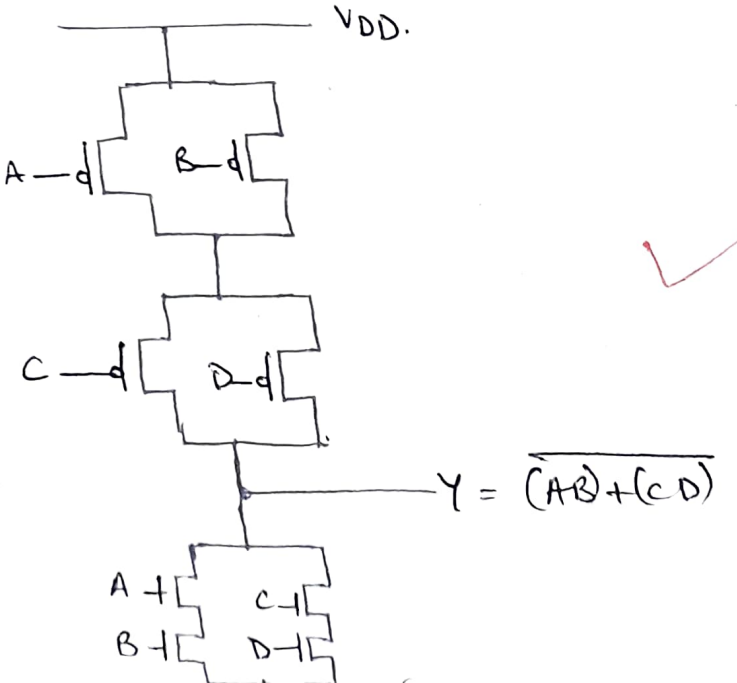
Q4) (a) $Y = \overline{(AB) + (CD)}$

nmos.
and - series
or - parallel

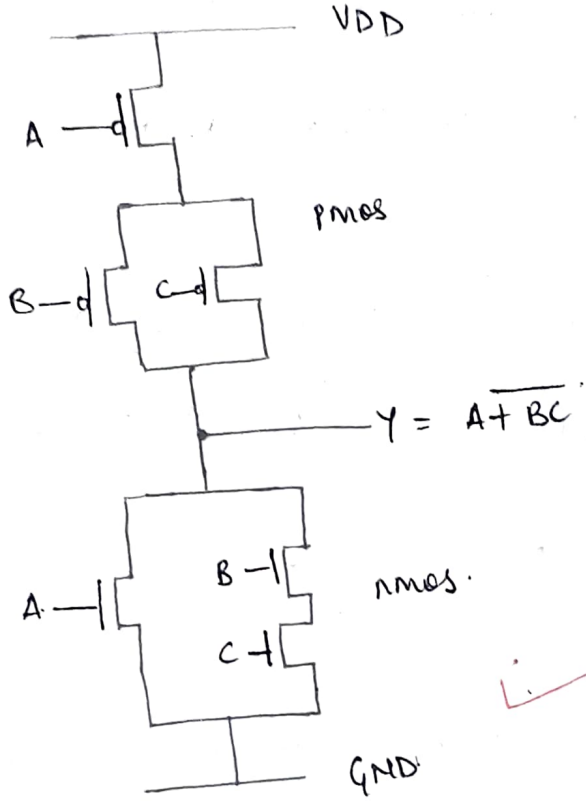
pmos.
and - parallel
or - series



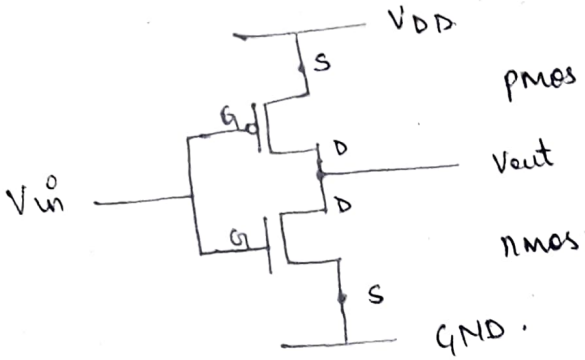
or.



(b) $Y = \overline{A + BC}$



Q5) ⇒ DC transfer characteristics of CMOS inverter relates to the output voltage to the input voltage.



CMOS structure

⇒ The threshold voltage of PMOS (V_{tp}) is always negative.
⇒ The threshold voltage of NMOS (V_{tn}) is always positive.

For nmos:

$V_{gsn} = V_g - V_s = V_{in} - 0 = V_{in}$

$V_{dsn} = V_d - V_s = V_{out} - 0 = V_{out}$

For pmos:

$V_{gsp} = V_g - V_s = V_{in} - V_{DD}$

$V_{dsp} = V_d - V_s = V_{out} - V_{DD}$

* Région de fonctionnement pour pmos and nmos:

for nmos:

$V_{gsn} < V_{tn} \longrightarrow$ cut-off région

$V_{gsn} > V_{tn} \longrightarrow$ either saturation or linear

$\longrightarrow V_{dsn} < V_{gsn} - V_{tn} \longrightarrow$ linear région

$\longrightarrow V_{dsn} \geq V_{gsn} - V_{tn} \longrightarrow$ saturation

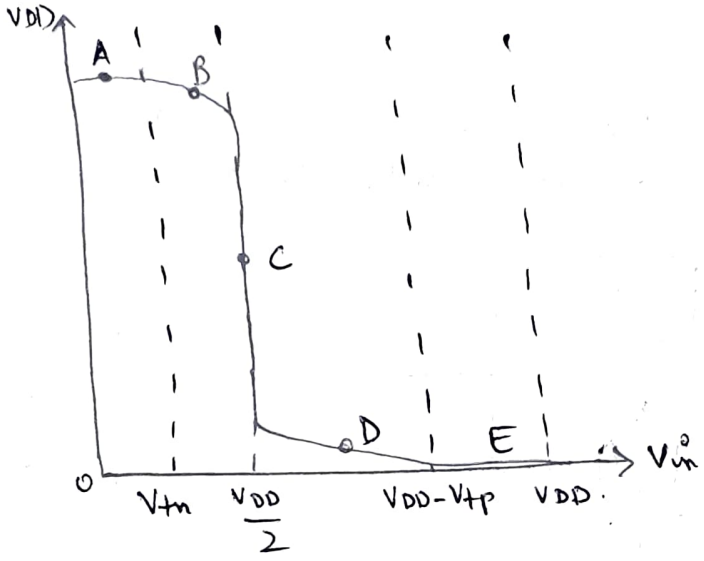
for pmos:

$V_{gsp} > V_{tp} \longrightarrow$ cut-off région

$V_{gsp} < V_{tp} \longrightarrow$ either saturation or cut-off

$\longrightarrow V_{dsp} > V_{gsp} - V_{tp} \longrightarrow$ linear région

$\longrightarrow V_{dsp} \leq V_{gsp} - V_{tp} \longrightarrow$ saturation



Region	nmos	pmos.
A	cut-off	linear
B	saturation	linear
C	saturation	saturation
D	linear	saturation
E	linear	cut-off.

In region A: pmos transistor is on and pulls the o/p to VDD nmos transistor is OFF. (cut-off region)

In region B: nmos transistor starts to turn ON, pulling the output down. (saturation region).

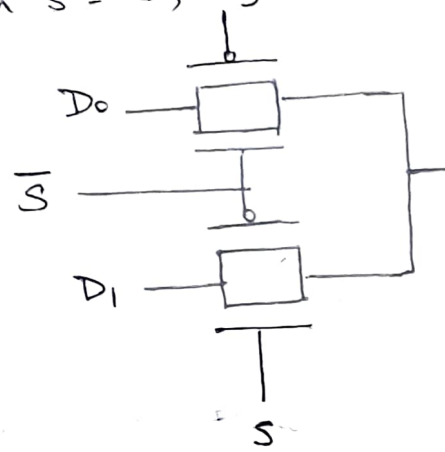
In region C: Both the transistors are in saturation region.

In region D: The pmos transistor is partially ON.

In region E: pmos transistor is OFF. Hence the nmos transistor drives / pulls the output down to 0.

8b) Transmission gate

In this example, selection line S=0 selects D_0 as the o/p and when S = 1, it selects D_1 as the i/p.

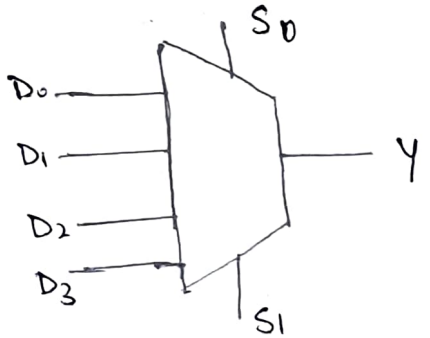


S	Y
0	D_0
1	D_1

This a transmission gate for a 2:1 MUX.

Incase of 4:1 MUX :

» There are 4 inputs and 2 selection lines. with 1



S_0 S_1	Y
0 0	D_0
0 1	D_1
1 0	D_2
1 1	D_3

& $S_1 = 0$.

» when $S_0 = 0$, the i/p D_0 is directed as output.

& $S_1 = 1$

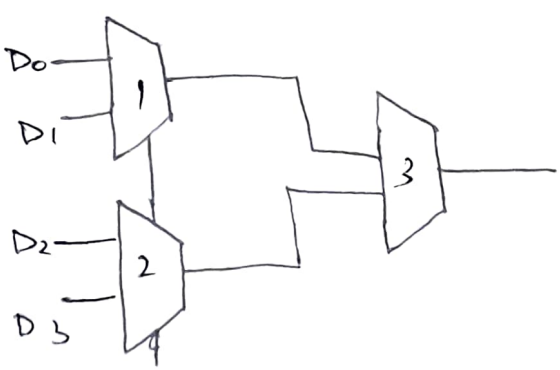
» when $S_0 = 0$, the i/p D_1 is selected and directed as o/p

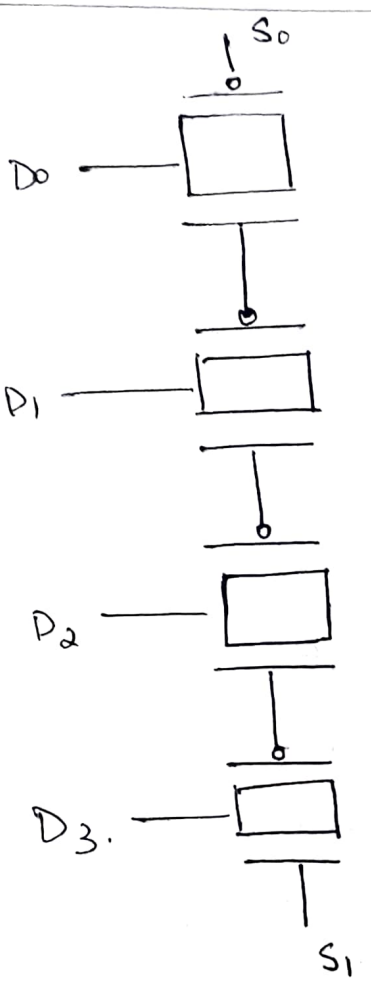
& $S_1 = 0$

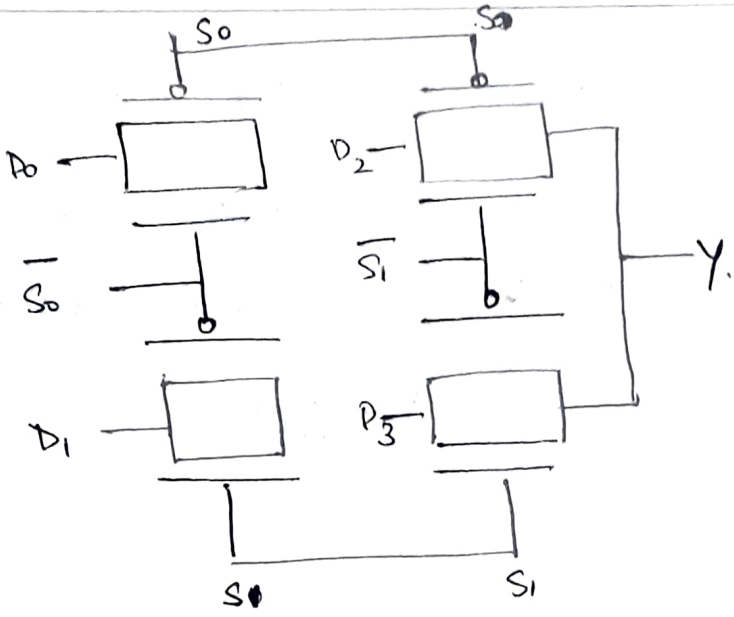
» when $S_0 = 1$, the i/p D_2 is selected and directed as o/

& $S_1 = 1$.

» when $S_0 = 1$, the i/p D_3 is selected and directed as o/

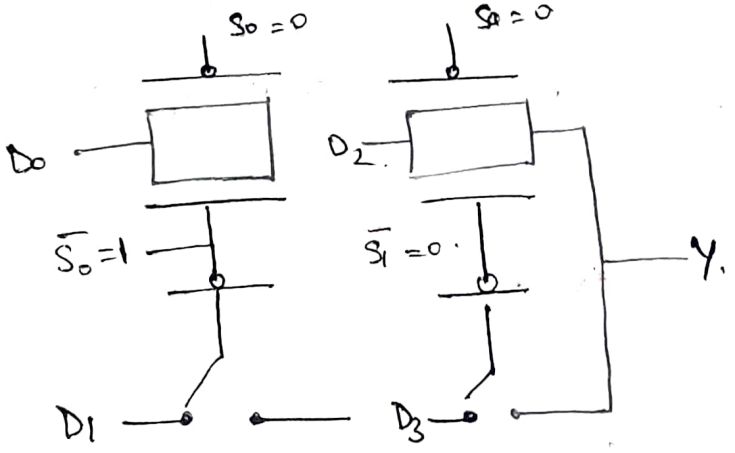






when $S_0 = 0$ & $S_1 = 0$.

i/p D_0 is selected and directed to o/p. Y.



when $S_0 = 0$ & $S_1 = 1$, i/p D_1 is selected and directed to the o