CMR INSTITUTE OF TECHNOLOGY

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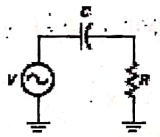
Internal Assesment Test - I

Sub:	Electronic Principles and Circuits						Code:	BEC303
Date:	19/12/2023	Duration:	90 mins	Max Marks:	50	Sem: 3rd	Branch:	ECE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Explain the different criteria's involved in VDB Analysis.	10	CO1	L2
2	Design the resistor values in a voltage divider bias to meet these specifications: VCC = 10 V , VCE @ midpoint , IC = 10 mA and β_{dc} =100 to 300.	10	CO1	L3
3	Discuss Emitter feedback bias and collector feedback bias.	10	CO1	L2
4	Derive voltage gain of common emitter amplifier from π model	10	CO1	L2

P.T.O

5	Explain the importance of coupling capacitor in base biased amplifier. if $R = 2k\Omega$ and the frequency range is from 20 Hz to 20 kHz, find the value of C needed to act as a good coupling capacitor in the below given Fig.5  Fig 5	10	CO1	L2
6	Explain in detail working of binary weighted resistor DAC with the neat circuit diagram	10	CO4	L2

CI CCI HOD

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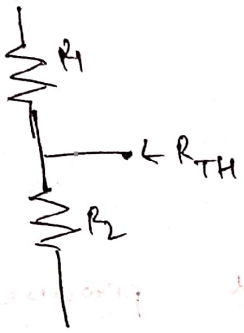
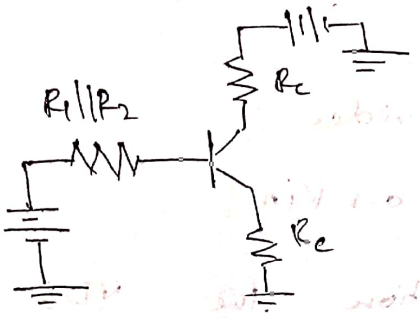
1. VDB or voltage divider bias is a circuit which has a stiff voltage divider at the input resistance of the transistor.



thevenin resistance



equivalent circuit

→ Thevenin Resistance

$$R_{TH} = R_1 || R_2$$

Because of this thevenin resistance the voltage of the VDB will not be ideal.
The current through the R_{TH} will reduce the voltage to base voltage from ideal voltage.

→ Accurat voltage divider

$$R_1 || R_2 < 0.01 R_{in}$$

A good VDB will follow this condition.

→ Stiff voltage divider

$$R_1 || R_2 < 0.01 R_{in}$$

$$R_{in} = \beta_{dc} R_e$$

$\therefore R_1 \| R_2 < 0.01 \beta_{dc} R_e$

The whenever possible, a designer will choose circuit values which follows these conditions. Hence the VDB will produce ultrastable Q point.

→ From voltage divider

$R_1 \| R_2 < 0.1 R_{in}$

Under this condition the VDB will produce reasonable Q-point

→ close approximation

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_1 \| R_2 / \beta_{dc}}$$

$R_1 \| R_2 = 10k\Omega \| 2.2k\Omega$

$= 1.8k\Omega$

$\beta_{dc} R_e = 200 \times 1k\Omega = 200k\Omega$

one-hundredth of $200k\Omega$

$\frac{1}{100} \times 200 \times 10^3 = 2k$

$\therefore 1.8k\Omega < 2k$ the VDB will act as a stiff VDB.

$$I_E = \frac{1.8V - 0.7}{1k + 1.8/200k} = \underline{1.094\ mA}$$

2. $V_{CC} = 10V$

V_{CE} @ midpoint

$I_C = 10mA$

$\beta_{dc} = 100$ to 300

$V_E = 10\%\ V_{CC}$

$= 0.01 \times 10$

$= 1V$

$I_E \approx I_C = 10mA$

$\therefore R_E = \frac{V_E}{R_E} = \frac{1}{10\ mA} = 100\Omega$

$R_C = 4R_E = .4 \times 100 = 400\Omega$

$R_2 < R_1$

$R_2 = 0.01 \beta_{dc} R_e$

$R_2 = 0.01(100)(100)$

$R_2 = 100\Omega$

$R_1 = \frac{V_1}{V_2} R_2 = \frac{8.3}{1.7} \times 100 = 488.23\Omega$

$= 490\Omega$

$V_2 = V_E + 0.7$

$= 1.7V$

$V_1 = V_{CC} - V_2$

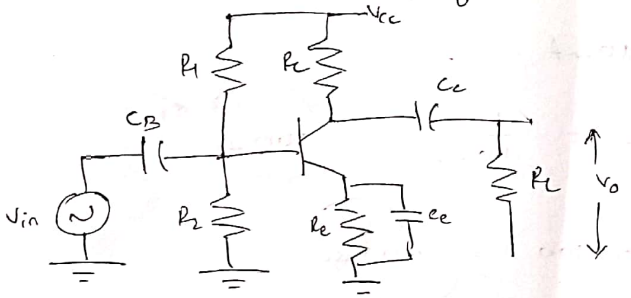
$= 10 - 1.87$

$= 8.3V$

∴ while designing a circuit which follows the given conditions,

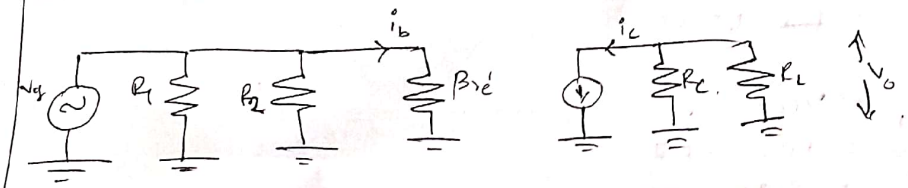
$R_1 = 490\Omega$
$R_2 = 100\Omega$
$R_E = 100\Omega$
$R_C = 400\Omega$

4. Common emitter amplifier



C_C → coupling capacitor
C_B → blocking capacitor
C_e → bypass capacitor
R_L → load resistance
V_{in} → input voltage
V_{cc} → DC input

π - model



$V_{in} = i\beta_{dc} r_e'$

$V_{out} = i_c (R_C \| R_L)$

∴ voltage gain i.e $A_v = \frac{V_{out}}{V_{in}}$

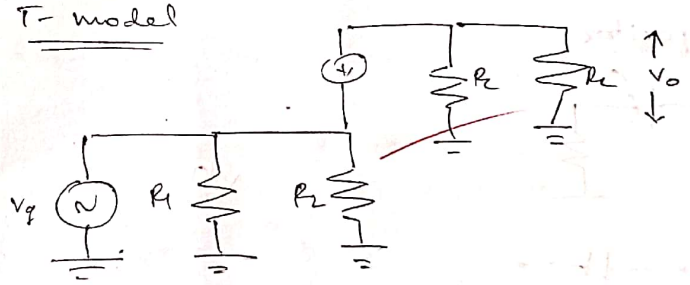
$$A_v = \frac{i_c (R_C \| R_L)}{i_b \beta_{dc} r_e'}$$

$$A_v = \frac{i_b \beta_{dc} (R_C \| R_L)}{i_b \beta_{dc} r_e'}$$

$R_C \| R_L \rightarrow r_e$ (equivalent resistance)

$$\boxed{A_v = \frac{r_C}{r_e'}}$$

T- model



$V_{in} = i_c r_c$

$V_{out} = i_e r_e'$

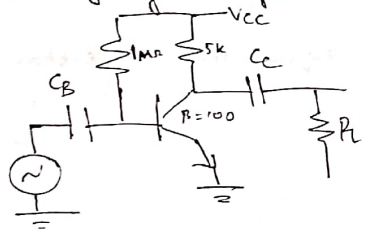
$i_c \approx i_e$

∴ voltage gain $A_v = \frac{V_{out}}{V_{in}} = \frac{i_e r_c}{i_c r_e'} = \frac{r_c}{r_e'}$

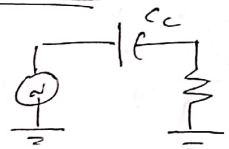
$$\boxed{A_v = \frac{r_c}{r_b}}$$

The above expression is same as the π-model because it is applicable to all transistors. Where the collector acts as an ac current source and emitter acts as a emitter resistance

5. A base biased amplifier is not much used in the industry but gives a basic idea about designing complicated circuits.



coupling capacitor



capacitor —||—

for dc quantities — open circuit

for Ac quantities — closed switch

- As the frequency increases the capacitive reactance decreases and becomes much smaller than the load resistance.

$$X_C = \frac{1}{2\pi fC}$$

$f \uparrow = X_C \downarrow$

- As a result input voltage appears across the load resistance.
- A capacitor that couples the input voltage with the output voltage is a coupling capacitor.
- A capacitor is an oper circuit for dc bias and not allow the current to leave the circuit.

$R = 2k\Omega$

f range = 20Hz to 20kHz

$C = ?$

from the expression: $X_C < 0.1R$ @ lowest frequency

$X_C < 0.1R$ @ 20Hz

$X_C < 0.1(2k)$ @ 20Hz

$X_C < 200\Omega$

$$C = \frac{1}{2\pi f X_C}$$

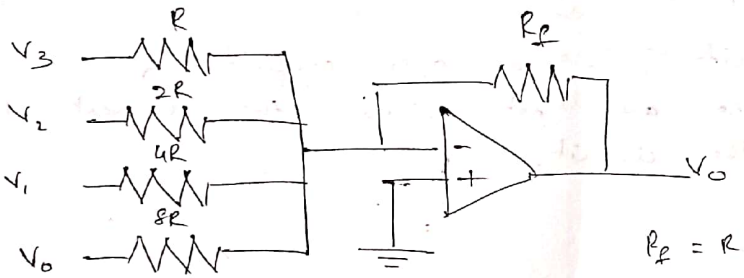
$$C = \frac{1}{2\pi f X_C}$$

$$C = \frac{1}{2\pi (20)(200)}$$

$C = 39.8\ \mu F$

Hence capacitance value of 39.8 μF will be needed to act as a good coupling capacitor given in the diagram.

6. Binary weighted resistor digital to analog converter.



$R_f = R = 1$

Voltage gain $A_{V_0} = -\frac{R_f}{8R} = \frac{1}{8} = -0.125$

Voltage gain $A_{V_1} = -\frac{R_f}{4R} = -\frac{1}{4} = -0.25$

Voltage gain $A_{V_2} = -\frac{R_f}{2R} = -\frac{1}{2} = -0.5$

Voltage gain $A_{V_3} = -\frac{R_f}{R} = -1$

total voltage gain

$V_o = V_{in} A_V$

$V_o = A_{V_0} V_0 + A_{V_1} V_1 + A_{V_2} V_2 + A_{V_3} V_3$

$V_o = -0.125 V_0 + -0.25 V_1 - 0.5 V_2 - V_3$

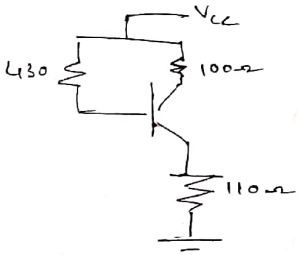
$\therefore V_o = -(V_3 + 0.5 V_2 + 0.25 V_1 + 0.125 V_0)$

8	4	2	1		
V_3	V_2	V_1	V_0		
0	0	0	0	→	0
0	0	0	1	→	−0.125V
0	0	1	0	→	−0.25V
0	0	1	1	→	−0.375V
0	1	0	0	→	−0.5V
0	1	0	1	→	−0.625V
0	1	1	0	→	−0.75V
0	1	1	1	→	−0.875V
1	0	0	0	→	−1V
1	0	0	1	→	−1.125V
1	0	1	0	→	−1.25V
1	0	1	1	→	−1.375V
1	1	0	0	→	−1.5V
1	1	0	1	→	−1.625V
1	1	1	0	→	−1.75V
1	1	1	1	→	−1.875V

- In binary weighted DAC, the output is not true analog, hence connected with a low pass filter to get a smooth curve at the output.

- This type of converter requires large number of different resistors as the number of inputs increases.
- Due to increase in number of resistors, loading effect will appear.
- This type of converter is used for limited inputs and where precision is not required.

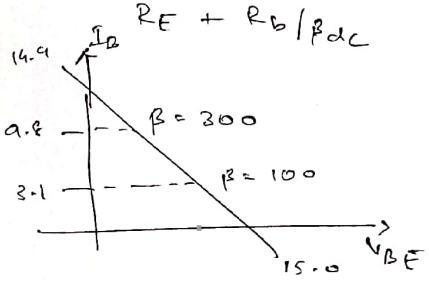
3. Emitter feedback bias



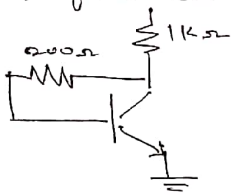
- Emitter feedback bias is a technique used in transistor amplifiers.
- A negative feedback is connected to the base where an attempt is made to neutralise the change in collector current.
- In this method the Q-point moves all over the load line due to transistor replacement and temperature changes.
- When the feedback is connected the q-points are stabilised by maintaining the temperature sensation and sensitivity of variation of other

transistor parameters.

$$I_E = \frac{V_{cc} - V_{BE}}{R_E + R_b/\beta_{dc}}$$



Collector feedback bias



- Also similar to emitter feedback bias to stabilize the Q-points.
- The main idea is to neutralise any change in collector current.
- In collector feedback biase, the negative feedback gives the voltage to the base where it reduces the change in original collector current

$$I_E = \frac{V_{cc} - V_{BE}}{R_c + R_b/\beta_{dc}}$$