IAT-03

(2) **Rise time:** It is the time taken to rise the voltage from to h

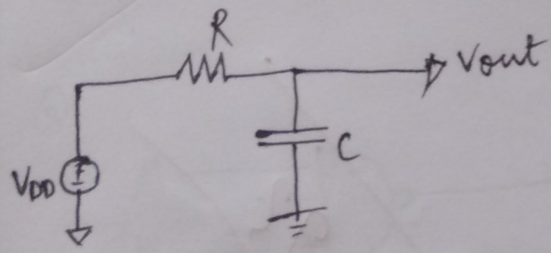
⇒ It is usually from 20% to 80% of the total voltag value in the graph.

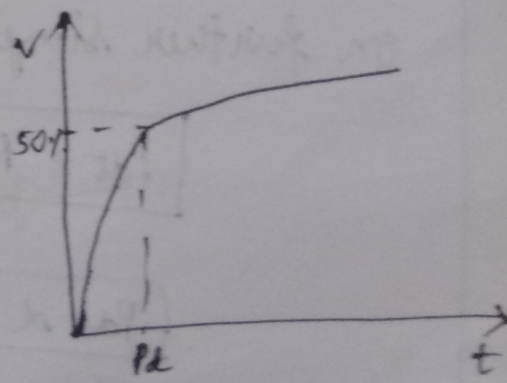
⇒ It can also be from 10% to 90%.

Fall time: It is the time taken by the inverter to fall from h High voltage to low voltage of a CMOS.

* It is usually from 80% to 20% of the total voltage value in the graph.
* But it can also be from 90% to 10%.

(3)





RC delay model shows a transient behaviour in the graph.

If we assume the transient function, the equation would b

$$H(S) = \frac{1}{1+SRC} \rightarrow (1)$$

on applying the inverse Laplace transform, the equation would be;

$$V_y(t) = V_{DD} \cdot e^{-t/\tau} \rightarrow (2)$$

where $\tau = RC$

For 1st order system, if we consider at $\frac{1}{2}$ time of V_{DD}, it; equal. Then;

$$V_y(t) = \frac{V_{DD}}{2} \rightarrow (3)$$

on substituting further in equations, we come across propagation delay Pdt time. we can substitute this in place of t.

$$\frac{V_{DD}}{2} = V_{DD} \cdot e^{-t/RC} \rightarrow (4)$$

on further simplification;

$$Pdt = RC \ln 2 \rightarrow (5)$$

$$Pdt \propto RC \rightarrow (6)$$

↳ propagation delay is directly proportional to the product RC.

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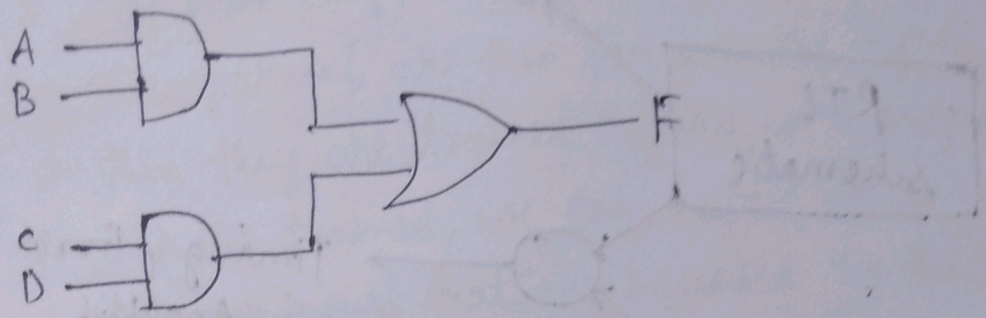
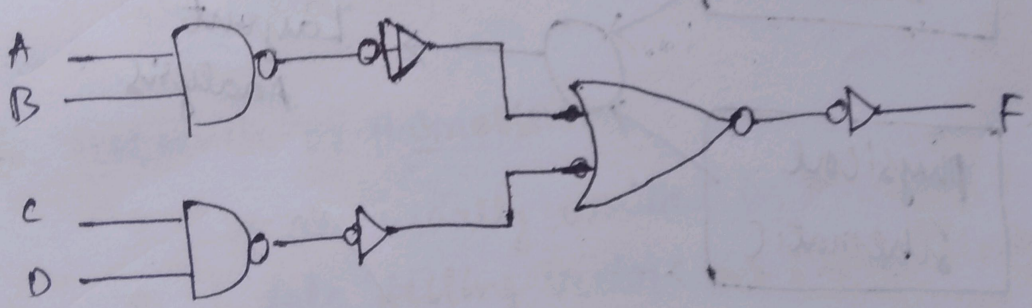
1

$F = AB + CD$

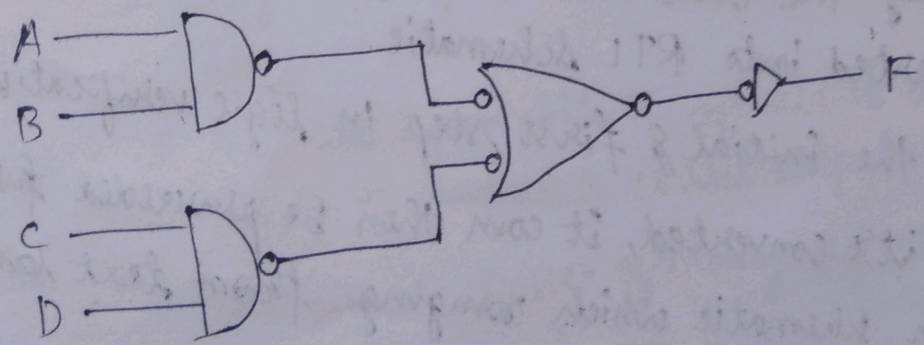
(1)



(2)



(3)



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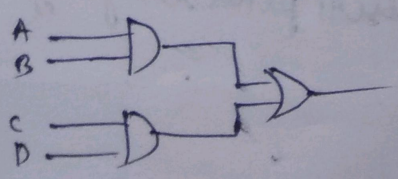
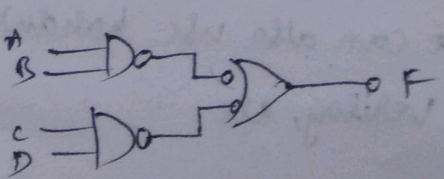
(4)



(5)



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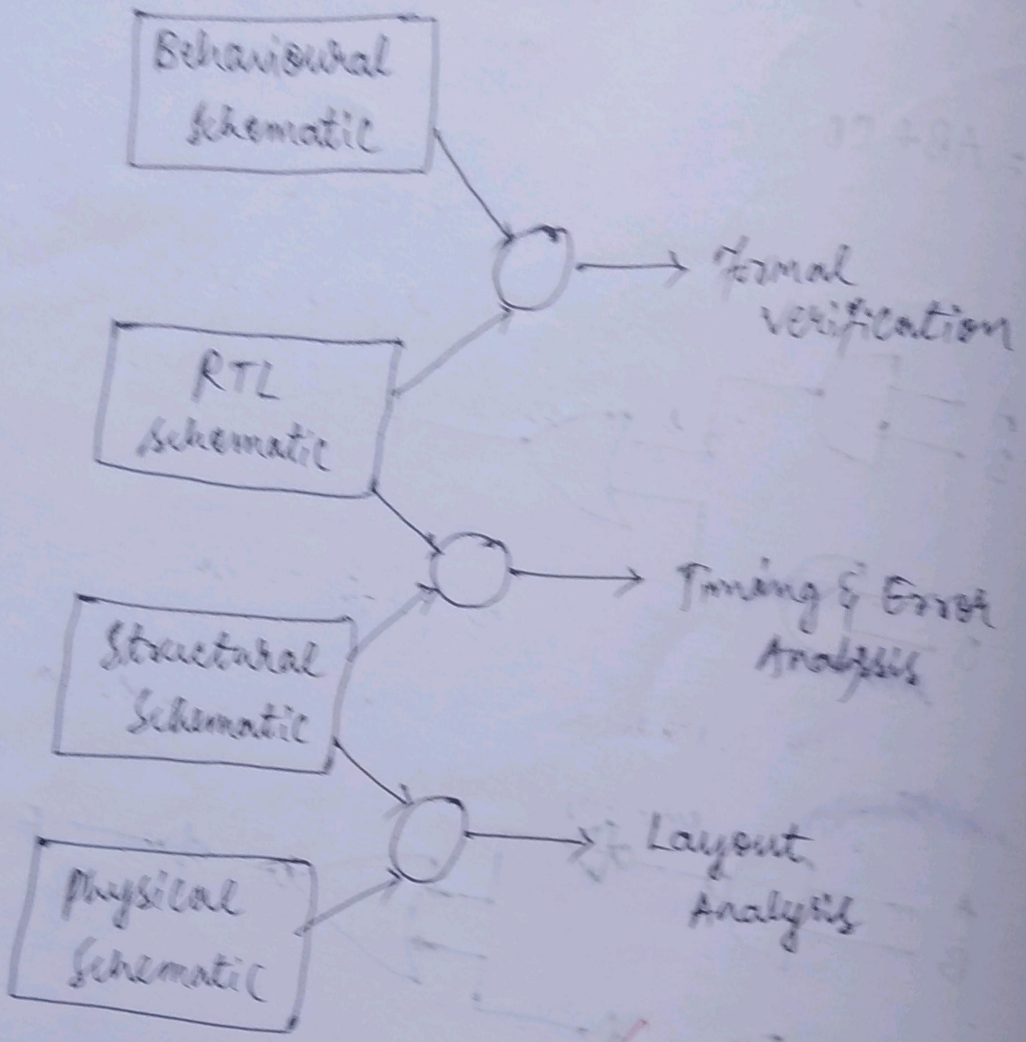

1. Initially the code that is in gate-level description will be converted into RTL schematic.
2. It is the initial & first step in logic verification.
3. once it's converted, it can then be proceeded further to other schematic which ranging from text languages high level languages like (C).
4. It can also use hardware description languages like HDL, verilog, etc.

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Logic verification principles

① Testing vectors:

* They form the patterns.
* These patterns are then fed into the inputs.
* Then they are trained together with outputs.
* Once it's trained, we can expect it to work on other inputs that are present in the IC.
* This is a basic principle on which other principles are based.

② Testbench or Harnessing.

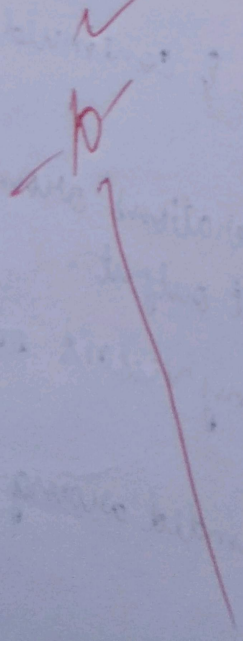
* They are usually written in HDL code.
* It take testing vectors as inputs along with it's own inputs.
* They are together trained & continued to further steps.
* These are like a bits of operations around IC that needs to produce a correct output.
* It's like a cluster of many vectors or circuits under test.
* These clusters are surrounded around the circuit for testing.

③ Double-checking:

* This includes many testbenches for simulation testing.
* It's like checking the outputs by comparing them with the expected ones.
* They are usually associated with Unix or Linux systems.

④ Bug Testing

* It finds all the errors in the above process.
* It finds the areas of problem and how big is the error or problem is.
* It gives an overall report of the problems that needs to be worked on.



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CMR

IAT-3

14 Logical effort is a ratio of input capacitance of a gate to the input capacitance of inverter which is the same output.

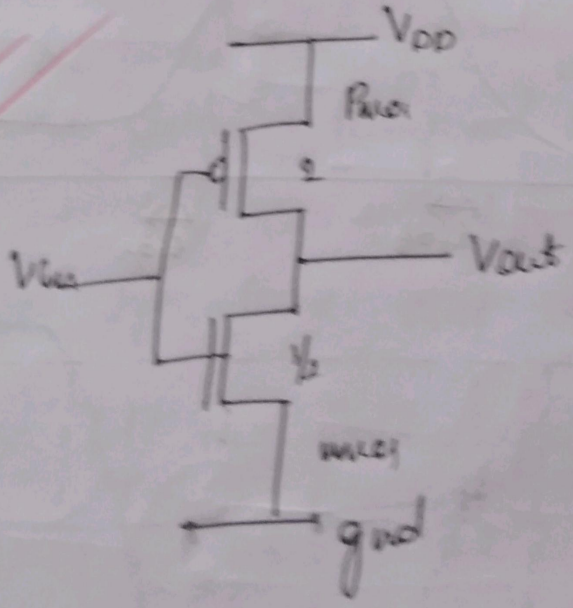
HI-skew inverter

skew inverter is given by

$\beta > 1$

$\beta_p > \beta_n$

$\left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)$



In normal inverter transistor sizing by

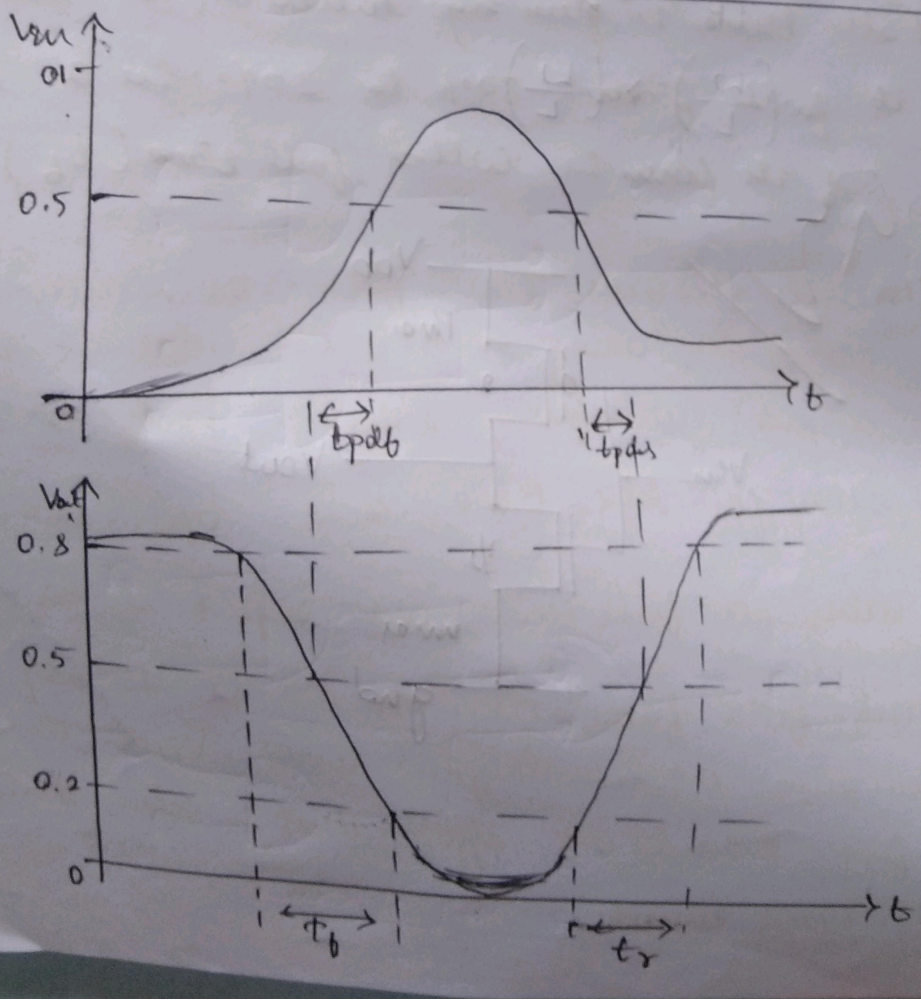
$W_{pmos} = 2$ and $W_{nmos} = 1$

But here in HI-skew inverter configuration by decreasing of NMOS transistor.

$W_{pmos} = 2$ & $W_{nmos} = 1/2$

Here, nmos value is reduced by factor 2 to construct decreasing nmos transistor

2)



→ The propagation delay is a time delay from the waveform of the input rising 50% to the output rising 50% is called propagation delay. It is denoted by t_{pd}

→ **Rise Time (t_r)**

Rise time is given by when in the waveform when it rise from 20% to 80% in steady state of waveform is called Rise time (t_r)

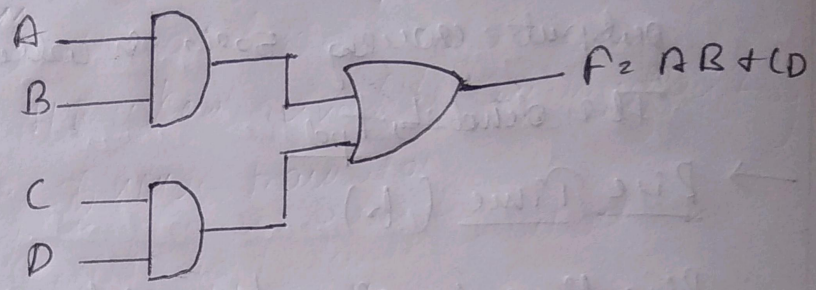
→ **Fall time (t_f)**

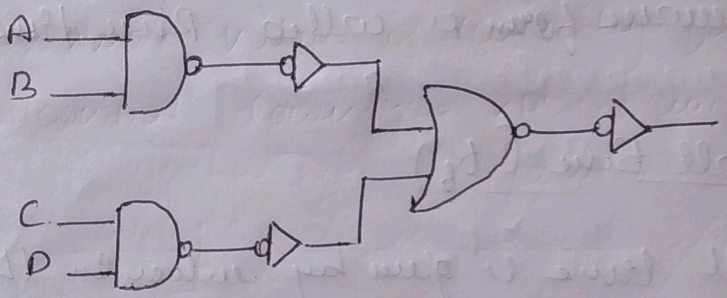
Fall time is given by when in the waveform when it falls from 80% to 20% in a steady state of the form is called fall time (t_f)

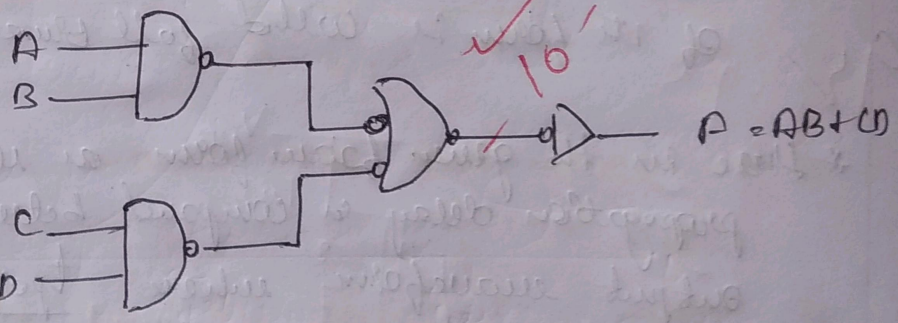
* Here in the given transfer characteristics the propagation delay is compared between input and output waveform where t_{pdf} is propagation delay for rise time and t_{pdr} is a propagation delay for fall time out input data.

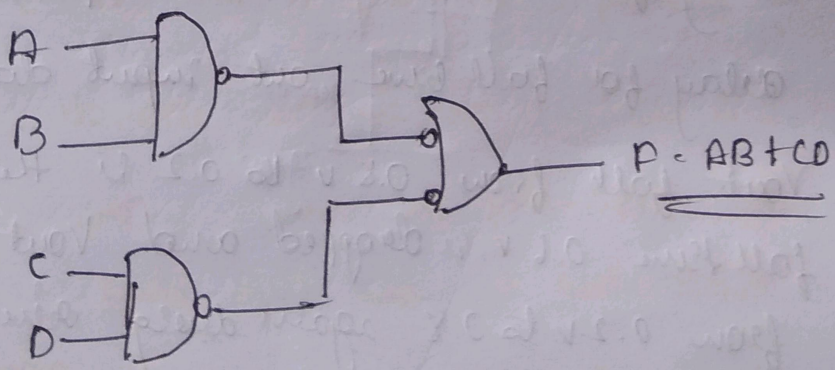
* Vout fall from 0.8 v to 0.2 v the t_f that during fall time 0.6 v is dropped and Vout start to increase from 0.2 v to 0.8 again during rise time of a CMOS inverter.

4) $F = AB + CD$









Bubble pushing

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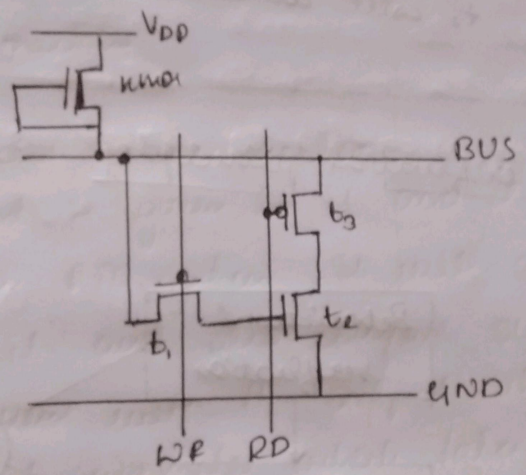
5) Static RAM is a type of ram or a temporary storage device which is used to store data even after the power is been cut. but it need to refresh continuously.

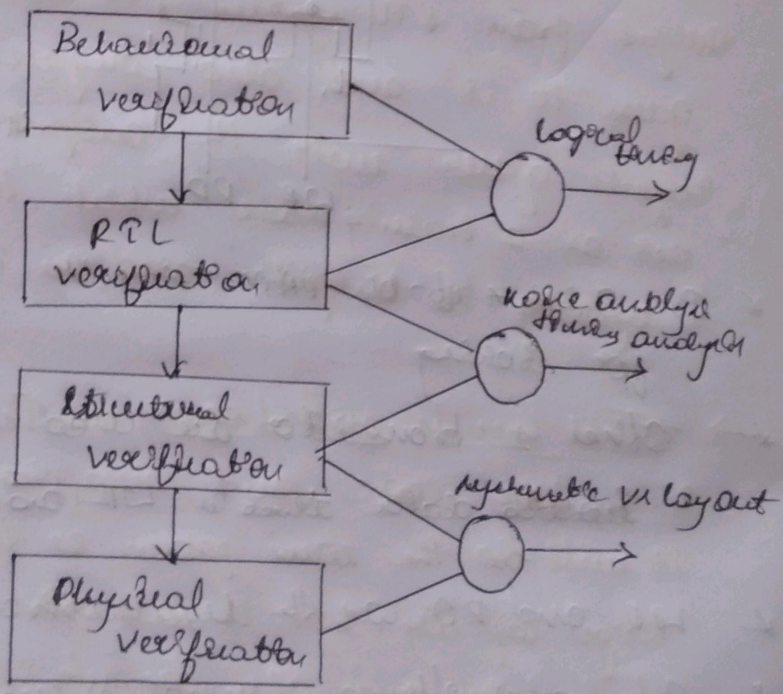
3 static RAM circuit



- In 3 ~~RAM~~ static RAM circuit 1 transistor is used for storing
- Other 2 transistor are used for reading and writing data through WR and RD.
- WR and RD are the two control line in 3 static RAM
- An external one nmos or CMOS circuit should be connected to the BUS line
- When t_1 and t_2 are ON the RAM will write the data

* When t_1 and t_3 are ON the CPU will read the data from memory.
* RD = Low, the BUS line will connected to bus and t_2 will be ON
* WR = high the BUS line will pass through t_1 which acts as participated
* WR = RD = Low both t_1 and t_3 will be short and only t_2 will conduct.

6) Logic verification principles



* The verification is the main and first process in designing logical circuits.
* The verification factor in a circuit depends on the RTL factor as it is a logic unit.

The verification principles are given by

* Test vector
* Test bench and harness
* Regression test
* Bug tracking

→ Test vector :- Test vector is a principle where the input is given to it and it already has the output from RTL system. It will analyse the inputs given to it and also compare output from the inputs given with the output already there. It acts as a tracing model which takes keeps on getting updating the outputs based on inputs.

→ Test bench and harness :- Test bench and harness is a HDL code and wrapped around a test vector. It will do the same process as test vector but in a larger capacity. Here it will also consider the output from test vector and also compute its own output. Harness means in a larger capacity with more accurately.

→ Regression test :- The a high level language script where it is able to output gate level verilog to RTL verification and also consider the output from test bench and analyse both outputs and give the final values.

→ Bug tracking :- Bug tracking is a process where it will try to find out the error or bug in the code, it will give the accurate location of error and also give the explanation why the error occured and also suggestions to correct error.

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