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Internal Assesment Test - III

Sub:	Electronic Principles and Circuits							Code:	BEC303
Date:	05/03/2024	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	ECE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Derive voltage gain and transconductance with necessary diagrams and equations of small signal analysis of MOSFETS.	10	CO1	L2
2	Explain the T equivalent circuit model of MOSFET with circuit diagram and suitable equations.	10	CO1	L2
3	Explain CS amplifier without source resistance with circuit diagram and suitable equations.	10	CO1	L2
4	Explain Class C Operation of power amplifier with circuit diagram and suitable equations.	10	CO2	L2

P.T.O

5	Explain the operation of UJT as relaxation oscillator suitable diagram and waveforms.	10	CO5	L2
6	Explain the operation of PUT with suitable symbol and circuit diagram.	10	CO5	L2

CI

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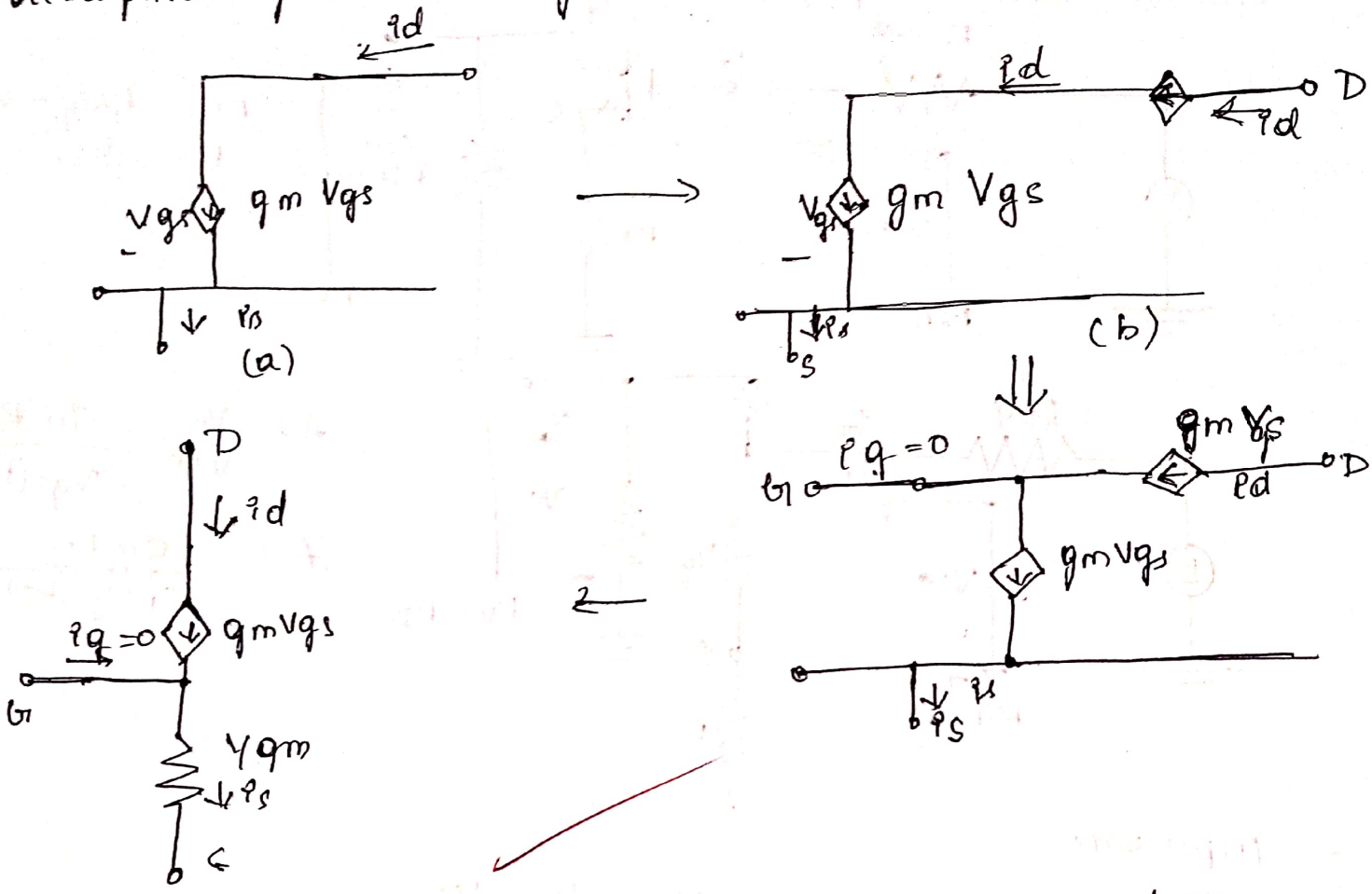
HOD

(2) By a simple transformation it is possible to develop an alternative equivalent circuit model for MOSFET. The development of such model for MOSFET. It mean as T model.



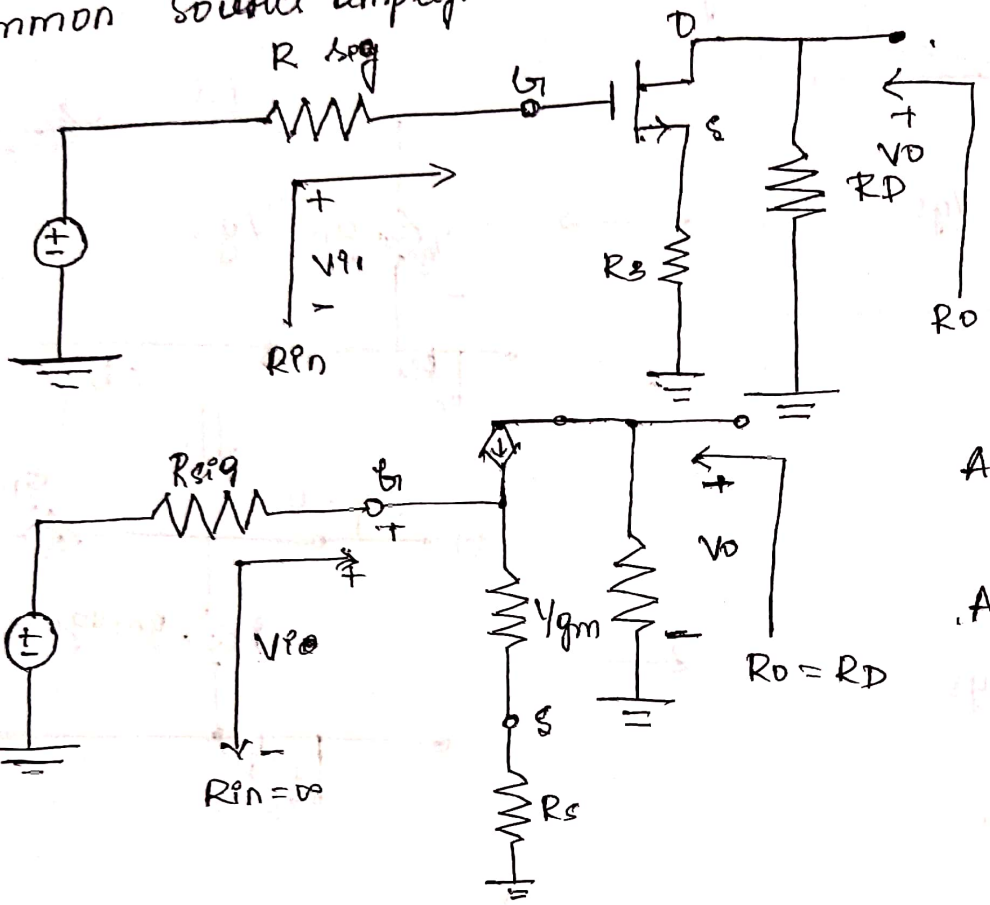
* This fig(a) shows equivalent circuit studied before without MOSFET.
* fig (b) we have added a second gm Vgs current source in series with the signal controlled source.
* This addition does not change the terminal curve.
* In fig (b) the X is the newly created circuit node formed at the gate terminal.
* In fig (c) the controlled curve source is (gm Vgs) connected to control voltage Vgs.

* We can replace the ~~controlled~~ controlled source by a resistor as long as the resistor draws the same current as the source the value of resistance

$$R_s \quad \frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$$

(3.) CS amplifier

Common source amplifier with a source resistance R_s



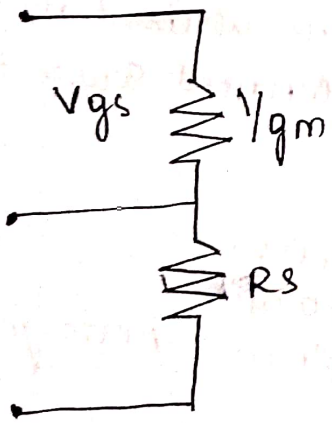
$R_{in} = R_{sig} = \infty$

$R_o = R_D$

$$A_V = \frac{V_o}{V_{in}} = \frac{-i_d R_D}{V_{gs}(1+g_m R_s)}$$

$$A_V = \frac{-g_m R_D}{(1+g_m R_s)}$$

Input side



$$V_{gs} = \frac{1/g_m \cdot V_i}{\frac{1}{g_m} + R_s}$$

$$V_{gs} = \frac{1}{1+g_m R_s} V_i$$

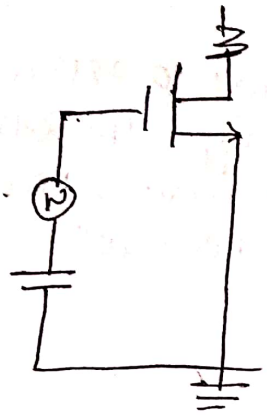
$$V_i = V_{gs}(1+g_m R_s)$$

To Ensure saturation region operation

$$V_D > V_{GS} - V_t$$

Since the total voltage at V_D the drain will have a signal component superimposed on V_D & V_D has to be sufficiently greater than $V_{GS} - V_t$ to allow for the required signal swing.

Since the total voltage at V_D the drain will have the signal



$V_{gs} \longrightarrow$ AC value

$V_{GS} \longrightarrow$ DC value

$V_{GS} \longrightarrow V_{gs} + V_{GS}$

$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{gs} - V_t)^2$$

$$g_D = \frac{1}{2} k_n \frac{W}{L} [V_{gs} - V_{GS}] - V_t]^2$$

$$[a+b-c]^2 = a^2 + b^2 + c^2 + 2ab - 2bc - 2ca$$

$$g_m = \frac{1}{2} k_n \frac{W}{L} [V_{GS}^2 + V_{gs}^2 + V_t^2 + 2V_{GS} V_{gs} - 2V_{GS} - V_t - 2V_t . V_{GS}]$$

Consider only AC components

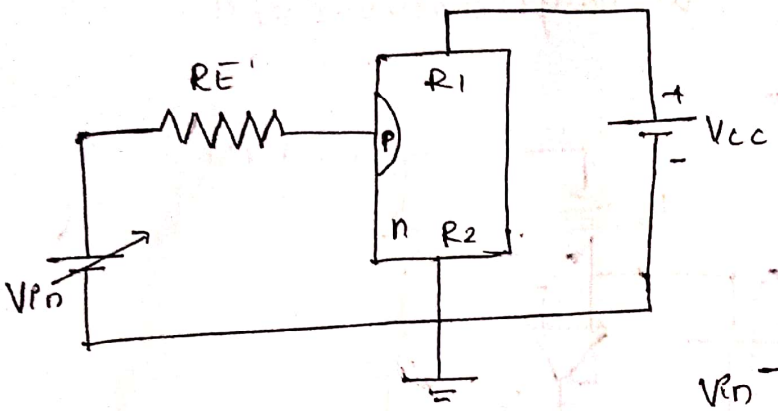
$$g_d = k_n \frac{W}{L} [V_{gs} (V_{GS} - V_t)]$$

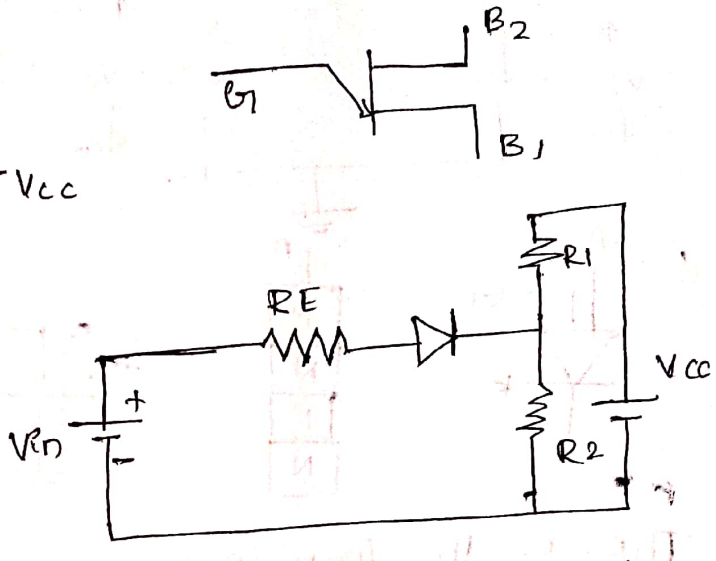
$$g_m = k_n \frac{W}{L} (V_{GS} - V_t]$$

$$A_V = g_m . R_D$$

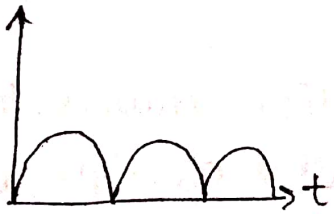
5.

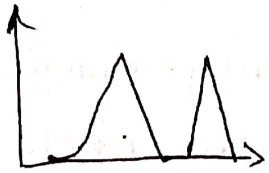
(5) UJT is used for generating pulse required for triggering circuit. It is also called as relaxation oscillator.



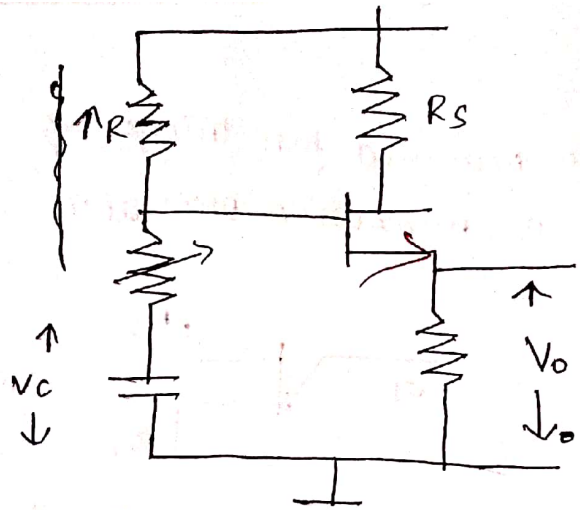


* UJT has two dopped region when the input voltage is zero device is non conducting
* When the input voltage is above the conduction standoff voltage of device
* The resistance b/w p region and lower n region becomes very small of UJT conduct.
* On the circuit capacitor charges towards V_{BB} when capacitor voltage reaches the standoff voltage V_{th} UJT turns on.
* Internal lower bar resistance quickly drops Allowing the capacitor to until low current drop
* The input voltage is above stand voltage UJT on VE resistance between the region and lower n region becomes very small and UJT conduct the UJT can be used to form a pulse generator circuit called as UJT relaxation oscillator.



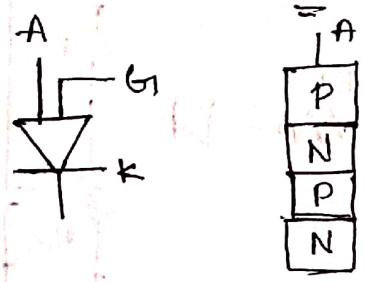


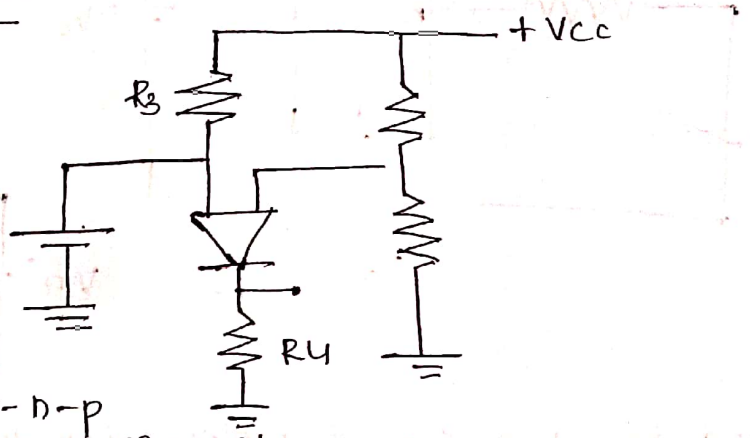
pulse for trigger.



In the ckt capacitor charge towards the V_{BB} when the capacitor voltage gives the UJT drop in value allowing capacitor discharge continous unit.

6.





circuit

There is the four layer p-n-p which is used to produce a trigger pulse and the waveform similar to UJT circuit. It's basic construction is different from UJT and more closely resembling an SCR.

The gate lead is connected to the n layer next to the anode the P-N junction is used to conduct.

The gate lead is connected to the N layer next to the anode. The gate voltage typically at ground point when the anode voltage become approximately 0.7V higher than the gate voltage the PUT turns off $V_A > 0.7V$ higher than the gate voltage.

The device will be remain on the until its anode current falls below.

The rated holding current

It is when the happens the device turns into - off state.

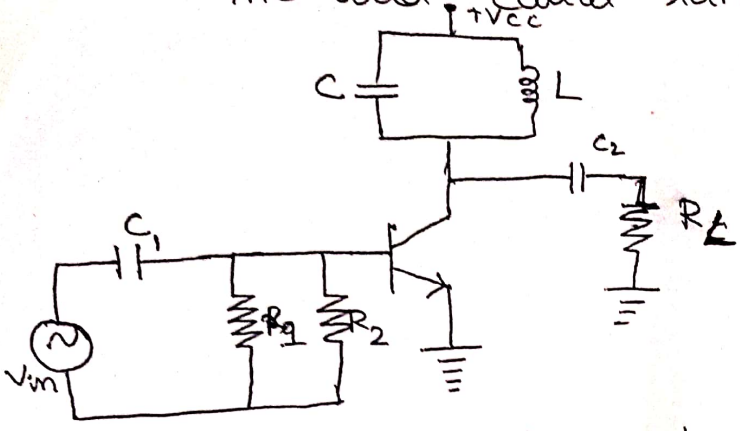
External resistance R_2 and R_3 establish gate lead is connected to the N layer.

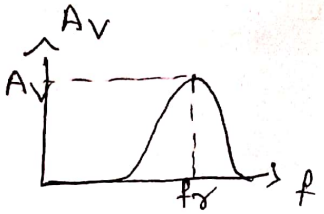
* PUT ⟶ Programmable unjunction transistor photo

SCR ⟶ The photo SCR also called as light activated sce

4. Explain class C operation of power amplifier with circuit diagram and suitable equations.

→ In class C operation it uses a resonant circuit for the load, called tuned oscillator.

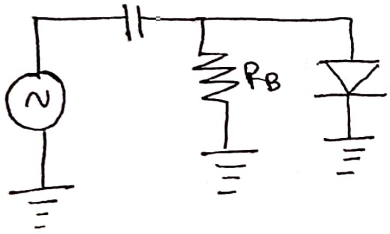


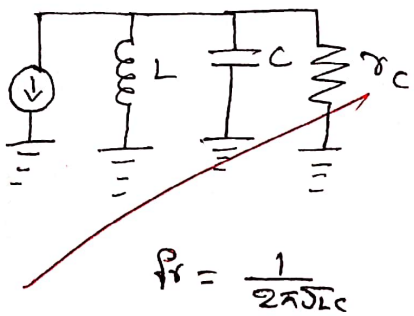


The V_{in} input voltage flows through the circuits and the output is seen in the collector. class c amplifier has a tank circuit. The collector current flows in +ve half cycle that is less than 180°

The efficiency will be very

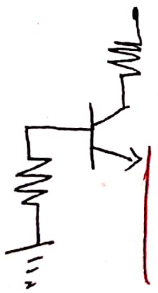
AC equivalent





DC equivalent

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$



- It helps to improve efficiency and reduces distortion.
- The inverted and amplified signal passed through the load R_L.

The Q point is at the lower end of the AC load line. when an AC signal is present, the instantaneous operating point moves up the AC load line towards the saturation point. The max pulse of collector current is given by the saturation current $(V_{cc}/r_c$

The voltage gain:

The total instantaneous drain voltage v_D as follows:

$$v_D = V_{DD} - R_D i_D \quad \text{—(1)}$$

under small signal conditions we have:

$$v_D = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as:

$$v_D = V_D - R_D i_d$$

Thus the signal component of drain voltage is $v_d = -i_d R_D = -g_m v_{gs} R_D$

which indicates that voltage gain is given by

$$A_v = \frac{v_d}{v_{gs}} = -g_m R_D \quad \text{—(A)}$$

The -ve sign in (A) as above indicates that o/p signal v_d is 180° out of phase w.r.t i/p signal.

The i/p signal must have magnitude lesser than $2(V_{GS} - V_t)$ to ensure linear operation.

* ——— * ——— *

The transconductance g_m:

$$g_m = k_n' \frac{W}{L} (V_{GS} - V_t) = k_n' (W/L) V_{ov} \quad -(1)$$

* This relationship of (1) indicates that g_m is proportional to process transconductance parameter $k_n' = \mu_n C_{ox}$ and W/L ratio of MOS transistor; hence to obtain relatively large transconductance the device must be short and wide.

* We observe that for a given device the transconductance is proportional to overdrive voltage.

$$V_{ov} = V_{GS} - V_t$$, the amount by which bias voltage V_{GS} exceeds the threshold voltage V_t.

* But increasing g_m by biasing the device at larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.

one useful expression is

$$g_m = \sqrt{2 k_n' \frac{W}{L} I_D} \quad -(2)$$

The (2) shows that:

1. For a given MOSFET, g_m is proportional to square root of dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.

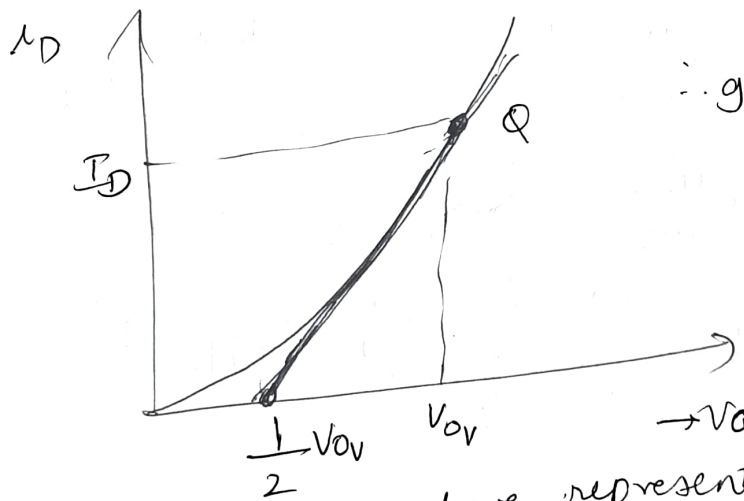
One more useful expression for g_m

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \quad -(3)$$

These are different relations for g_m, for determining g_m with 3 design parameters (W/L), V_{OV} and I_D. any of two of which can be chosen independently

* That is the designer may choose to operate the MOSFET with a certain overdrive voltage V_{OV} and at a particular current I_D, the required W/L ratio can then be found and the resulting g_m determined

* ——— * ——— * ———



$$\therefore g_m = \frac{I_D}{\frac{1}{2}V_{OV}}$$

The graph above represents (3) above)