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Internal Assesment Test - III

Sub:	Computer Organization and Architecture							Code:	BEC306C
Date:	05/03/2024	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	ECE
Answer Any FIVE FULL Questions									

		Marks	OBE	
			CO	RBT
1.	With the help of necessary diagrams explain the internal organization of a 16*8 bit RAM chip.	[10]	CO3	L2
2.	With a neat sketch, explain a method for handling interrupts from multiple devices.	[10]	CO3	L2
3.	Write notes on i)ROM,ii)PROM, iii)EPROM, iv) EEPROM, v)Flash memory	[10]	CO3	L2
4.	With a neat diagram, explain DMA controller.	[10]	CO3	L2

PTO

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5.	With the help of single bus organisation of data path inside a processor explain the steps followed by the processor to execute an instruction.	[10]	CO4	L2
6.	a) Explain gating signals associated with MDR. Give necessary diagrams.	[05]	CO4	L2
	b) Give control sequence for the execution of instruction ADD (R2),R1	[05]	CO4	L2
7.	With a block diagram, describe the three bus organization of the datapath inside a processor. Give the control sequence forexecution of the instruction ADD R3,R2.R1	[10]	CO4	L2
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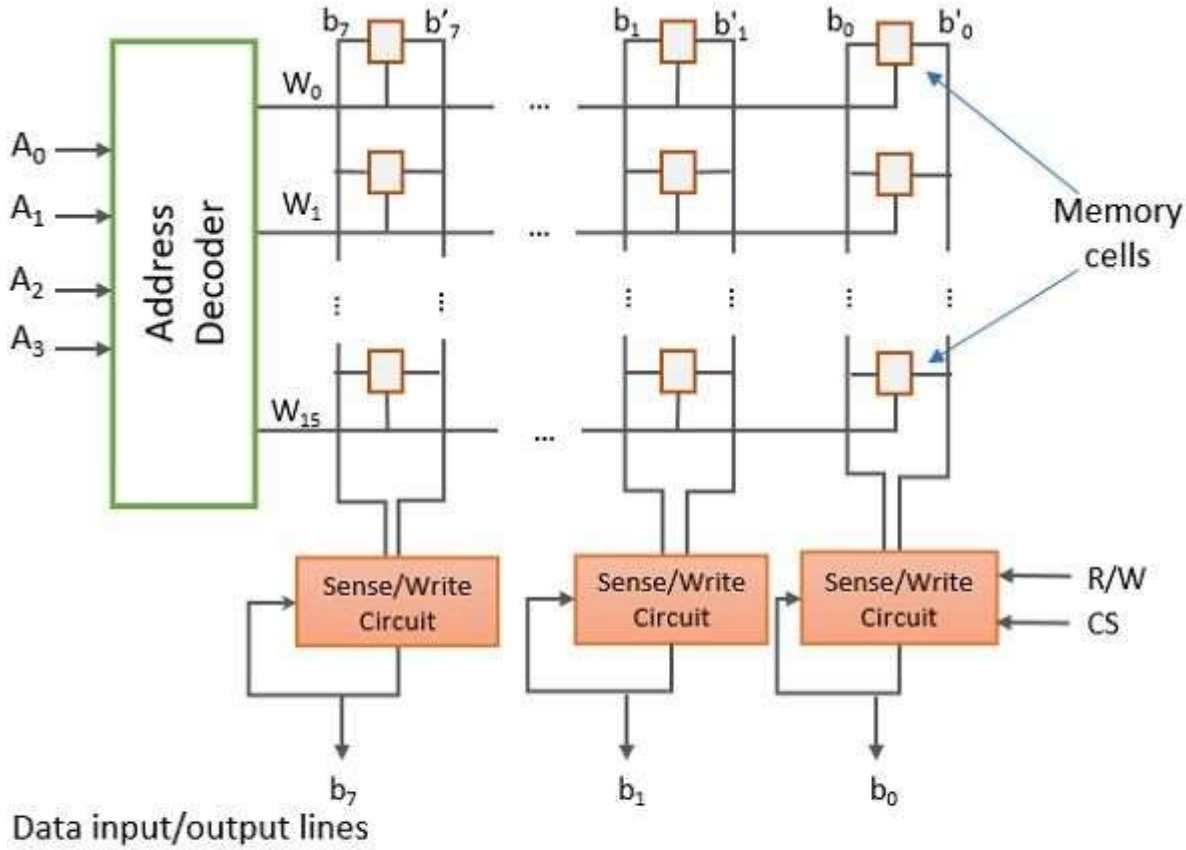
Solutions

1. With a neat diagram, explain the organization of 2M X 8 dynamic memory chip. Organized as 4kx4k array. 4096 cells in each row are divided into 512 groups of 8. Each row can store 512 bytes. 12 bits to select a row, and 9 bits to select a group of 8 bits in a row. Total of 21 bits. (2 MB). Reduce the number of bits by multiplexing row and column addresses. First apply the row address, RAS signal latches the row address. Then apply the column address, CAS signal latches the address. Timing of the memory unit is controlled by a specialized unit which generates RAS and CAS. This is asynchronous DRAM.
   - All the contents of a row are selected based on a row address.Particular byte is selected based on the column address. - Add a latch at the output of the sense circuits in each row. All the latches are loaded when the row is selected. Different column addresses can be applied to select and place different bytes on the data lines. - Consecutive sequence of column addresses can be applied under the control signal CAS, without reselecting the row. Allows a block of data to be transferred at a much faster rate than random accesses. A small collection/group of bytes is usually referred to as a block. This transfer capability is referred to as the fast page mode feature.



Organization of Memory Cells on Semiconductor Memory Chip

2. What is ROM memory? What are the different types of ROM. Explain? Read-Only Memory: Data are written into a ROM when it is manufactured. Programmable Read-Only Memory (PROM): Allow the data to be loaded by a user. Process of inserting the data is irreversible. Storing information specific to a user in a ROM is expensive. Providing programming capability to a user may be better. Erasable Programmable Read-Only Memory (EPROM): Stored data to be erased and new data to be loaded. Flexibility, useful during the development phase of digital systems. Erasable, reprogrammable ROM. Erasure requires exposing the ROM to UV light. Electrically Erasable Programmable Read-Only Memory (EEPROM): To erase the contents of EPROMs, they have to be exposed to ultraviolet light. Physically removed from the circuit. EEPROMs the contents can be stored and erased electrically Flash memory: It is similar approach to EEPROM. Read the contents of a single cell, but write the contents of an entire block of cells. Flash devices have greater density. Higher capacity and low storage cost per bit. Power consumption of flash memory is very low, making it attractive for use in equipment that is battery-driven. Single flash chips are not sufficiently large, so larger memory modules are implemented using flash cards and flash drives.

3.

Handling Multiple devices

The information needed to determine whether a device is requesting an interrupt is available in its status register. When a device raises an interrupt request, one of the bits of the status register is set to 1 which we call IRQ bit.

KIRQ, DIRQ are the interrupt request bits for keyboard and display. The polling scheme ha the disadvantage that the time spent interrogating the IRQ bits of all the devices that may not be requesting any service. An alternate approach is to use vectored interrupts.

Vectored Interrupts

A device requesting an interrupt can identify itself by sending special code to the processor over the bus. The code supplied by the device represents the starting address of the interrupt service routine. The code length is 4 to 8 bits. The processor reads this address called the interrupt vector and stores it in to the PC. The interrupt vector may also include a new value for a processor status register.

The interrupted device must wait to put on the bus only when the processor is ready to receive it. When the processor is ready to receive the vector interrupt code, it activates the interrupt acknowledge line INTA. The I/O device responds by sending its interrupt vector code and turning off INTR signal.

Interrupt Nesting

I/O devices should be organized in a priority structure. An interrupt request from a high priority should be accepted while the processor is serving another request from the lower priority device.

We can assign priority level to the processor that can be changed under program control. The priority level of the processor is the priority of the program that is currently being executed. The processor accepts interrupts from devices that have priorities higher than its own.

The processor is in supervisory mode when it is executing the OS routines. It switches to User mode before beginning to execute application programs. The privileged instructions can be executed only while the processor is running in the supervisory mode. A multiple priority scheme can be implemented by using separate interrupt request and interrupt acknowledge lines from each device.

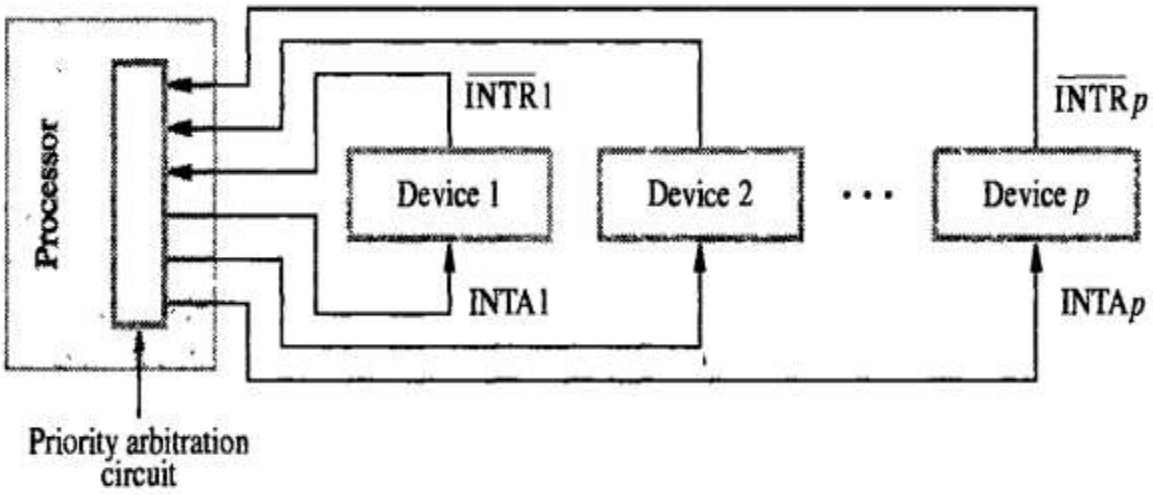


Fig 6: Implementation of interrupt priority using individual interrupt request & acknowledge lines

4.

Direct Memory Access

To transfer large blocks of data at high speeds, an alternate approach is used. A special control unit may be provided to allow transfer of block of data directly between external device and main memory without intervention by processor. This approach is called direct memory access or DMA.

DMA transfers are performed by control circuits that are part of I/O interface called DMA controller. The DMA controller performs functions that would normally be carried out by processor when accessing main memory.

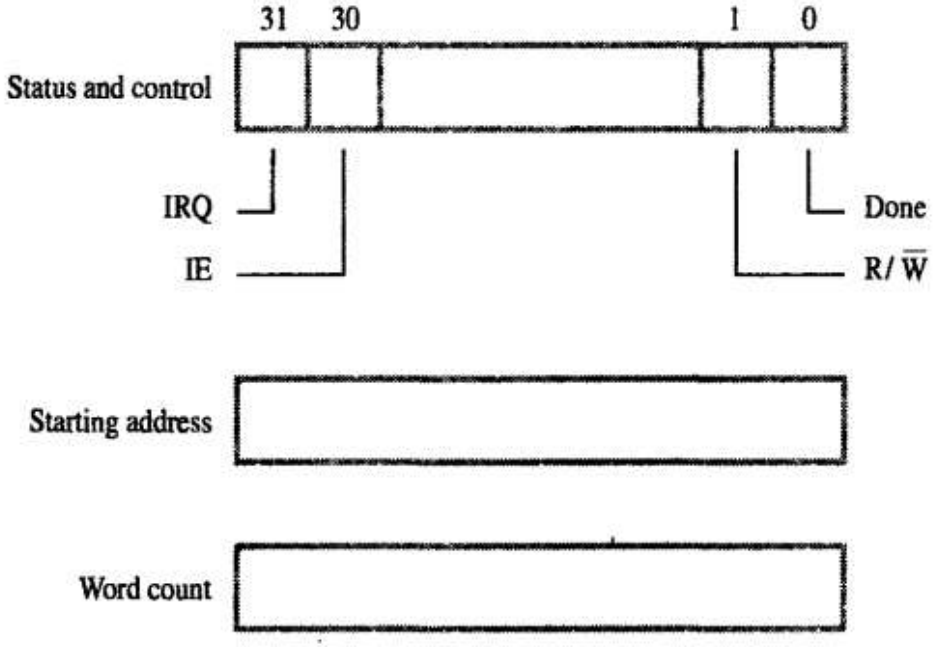


Fig 9: Registers in DMA interface

The R/$\overline{W}$ bit determine the direction of transfer. When this bit is set to 1 by a program instruction, the controller performs read operation that is it transfers data from memory to I/O device. When transfer is complete, it sets done flag to 1. When IE is1, it causes the controller to raise an interrupt after it has completed transferring block of data. Finally IRQ bit is set to 1 when it has requested interrupt.

Requests from DMA devices are given high priority than processor requests. Among different DMA devices high priority is given to high speed peripherals such as disks, high speed network interface or graphic display device.

The processor originates most memory cycles, the DMA controller is said to steal memory cycles from processor. This technique is called cycle stealing. DMA controller is given access to main memory to transfer a block of data without interruption. This is called as block or burst mode.

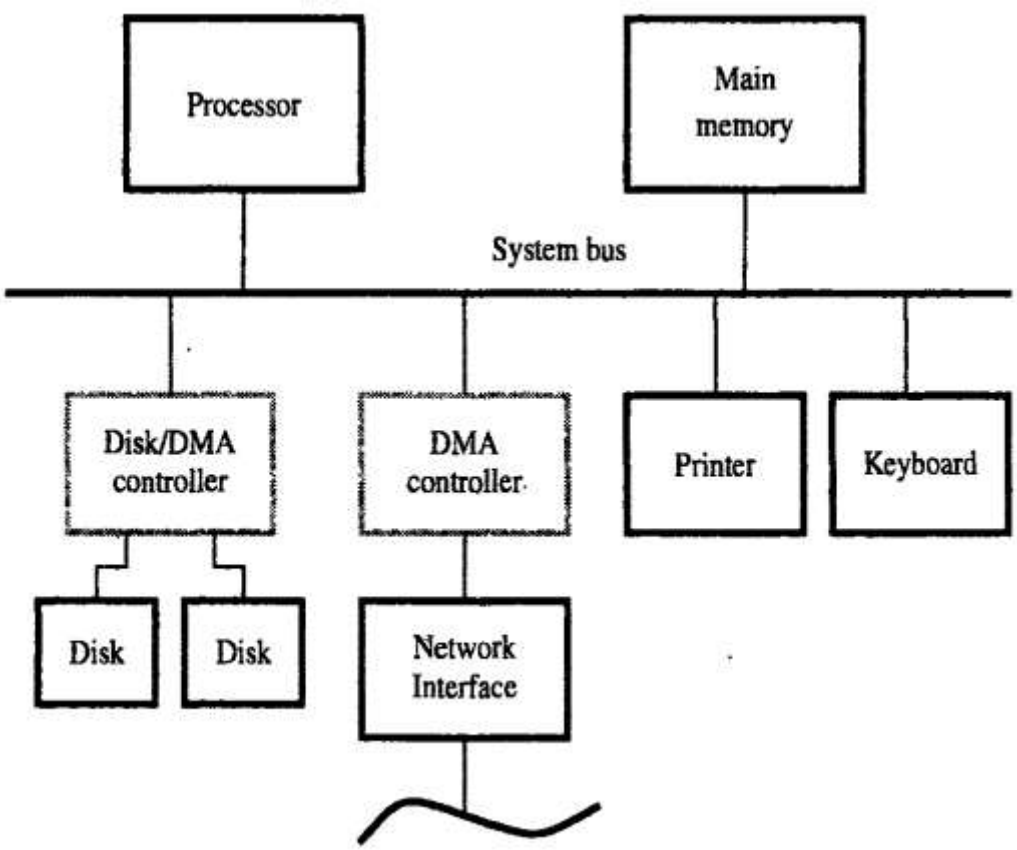
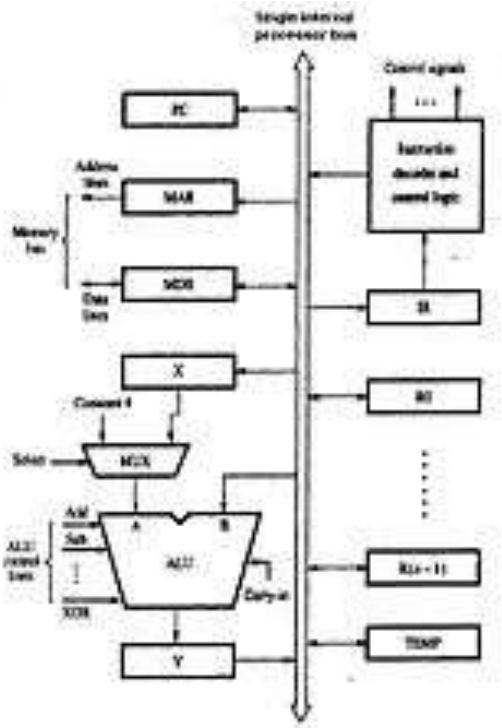


Fig 10: Use of DMA controllers in computer system

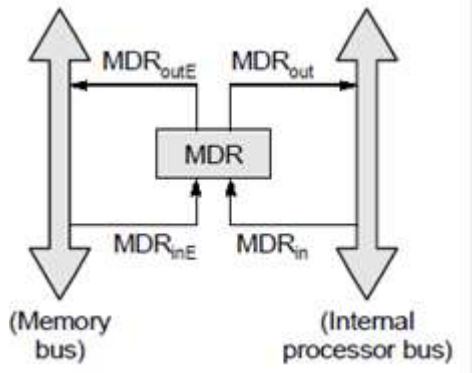
5.



Single Bus Organization

- Single bus organization contains MAR, MDR registers. MDR has two inputs and two outputs. Data may be loaded into MDR wither from the memory bus or from the internal processor bus. Data stored in MDR may be place on either bus. - The input of MAR is connected to the internal bus, and its output is connected to the external bus. - The control lines of the memory bus are connected to the instruction decoder and control logic block. - Three registers: Y, Z and Temp are used in this design. - ALU must have only one input connection from the bus. The other input must be stored in a holding register called Y register. - A multiplexer selects among register Y and 4 depending upon select line. One operand of a two-operand instruction must be placed into the Y register before the other operand must be placed onto the bus. Identical reasoning tells us that there must be an output register Z which collects the output of the ALU at the end of each cycle. - This way, there can be one operand in the Y register, one operand on the bus and the result stored in the Z register - The register, ALU and the interconnecting bus are collectively referred as datapath. - The following sequence are considered for instruction execution - Transfer a word of data from one processor to another or to the ALU - Perform an arithmetic or logic operation and store the result - Fetch the contents of a given memory location and load them into processor register - Store a word of data from a processor register into a given memory location

6. A)



• To fetch instruction/data from memory, processor transfers required address to MAR (whose output is connected to address-lines of memory-bus). At the same time, processor issues Read signal on control-lines of memory-bus. • When requested-data are received from memory, they are stored in MDR. From MDR, they are transferred to other registers • MFC (Memory Function Completed): Addressed-device sets MFC to 1 to indicate that the contents of the specified location → have been read & → are available on data-lines of memory-bus

6 B) EXECUTION OF A COMPLETE INSTRUCTION

• Consider the instruction Add (R3),R1 which adds the contents of a memory-location pointed by R3 to register

R1. Executing this instruction requires the following actions:

1) Fetch the instruction.
2) Fetch the first operand.
3) Perform the addition.
4) Load the result into R1.

• Control sequence for execution of this instruction is as follows

1) PCout, MARin, Read, Select4, Add, Zin
2) Zout, PCin, Yin, WMFC
3) MDRout, IRin
4) R3out, MARin, Read
5) R1out, Yin, WMFC
6) MDRout, SelectY, Add, Zin
7) Zout, R1in, End

• Instruction execution proceeds as follows:

Step1--> The instruction-fetch operation is initiated by loading contents of PC into MAR & sending a Read request to memory. The Select signal is set to Select4, which causes the Mux to select constant 4. This value is added to operand at input B (PC‟s content), and the result is stored in Z

Step2--> Updated value in Z is moved to PC.

Step3--> Fetched instruction is moved into MDR and then to IR.

Step4--> Contents of R3 are loaded into MAR & a memory read signal is issued.

Step5--> Contents of R1 are transferred to Y to prepare for addition.

Step6--> When Read operation is completed, memory-operand is available in MDR, and the addition is performed.

Step7--> Sum is stored in Z, then transferred to R1.The End signal causes a new instruction fetch cycle to begin by returning to step1

7. • All general-purpose registers are combined into a single block called the register file.

• Register-file has 3 ports. There are 2 outputs allowing the contents of 2 different registers to be simultaneously
placed on the buses A and B.

• Register-file has 3 ports.

1) Two output-ports allow the contents of 2 different registers to be simultaneously placed on buses A & B.
2) Third input-port allows data on bus C to be loaded into a third register during the same clock-cycle.

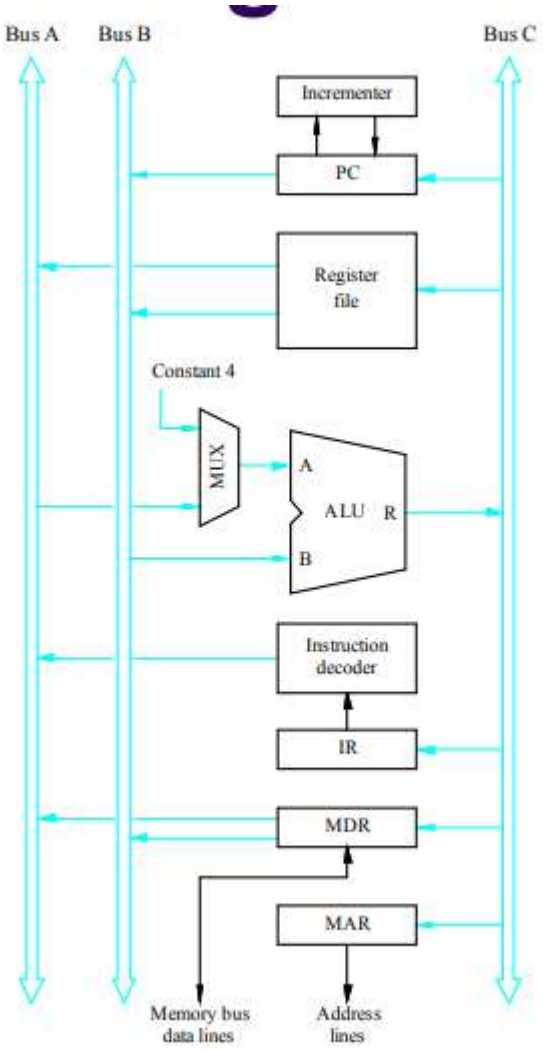
• Buses A and B are used to transfer source-operands to A & B inputs of ALU.
• Result is transferred to destination over bus C.
• Incrementer-unit is used to increment PC by 4.
• Control sequence for the instruction Add R4,R5,R6 is as follows

1) PCout, R=B, MARin, Read, IncPC
2) WMFC
3) MDRout, R=B, IRin
4) R4outA, R5outB, SelectA, Add, R6in, End

• Instruction execution proceeds as follows:

Step 1--> Contents of PC are passed through ALU using R=B control-signal and loaded into

MAR to start a memory Read operation. At the same time, PC is incremented by 4.
Step2--> Processor waits for MFC signal from memory.
Step3--> Processor loads requested-data into MDR, and then transfers them to IR.
Step4--> The instruction is decoded and add operation take place in a single step.



8.

9.

HARDWIRED CONTROL

- Decoder/encoder block is a combinational-circuit that generates required control-outputs depending on state of all its inputs.
- Step-decoder provides a separate signal line for each step in the control sequence.
  Similarly, output of instruction-decoder consists of a separate line for each machine instruction.
- For any instruction loaded in IR, one of the output-lines INS_1 through INS_m is set to 1, and all other lines are set to 0.
- The input signals to encoder-block are combined to generate the individual control-signals Y_{in}, PC_{out}, Add, End and so on.
- For example, $Z_{in}=T_1+T_6.ADD+T_4.BR$;This signal is asserted during time-slot T_1 for all instructions,
  during T_6 for an Add instruction
  during T_4 for unconditional branch instruction
- When RUN=1, counter is incremented by 1 at the end of every clock cycle.
  When RUN=0, counter stops counting.
- Sequence of operations carried out by this machine is determined by wiring of logic elements, hence the name "hardwired".
- Advantage: Can operate at high speed.
  Disadvantage: Limited flexibility.

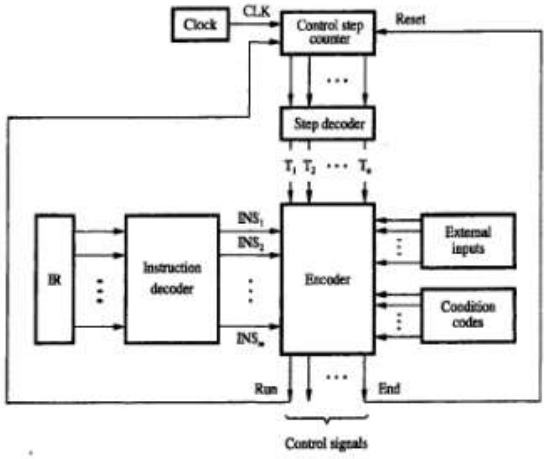


Figure 7.11 Separation of the decoding and encoding functions.