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CMR INSTITUTE OF TECHNOLOGY

Internal Assessment Test 2 – Jan 2024

Sub:	**Digital Design and Computer Organization**					Sub Code:	**BCS302**	Branch:	**AIML**
Date:	**18/1/2024**	Duration:	**90 minutes**	Max Marks:	**50**	Semester	**III**		**OBE**

		Answer any FIVE Questions	**MARKS**	**CO**	**RBT**
1		Design a full adder by constructing the truth table and simplify the output equations.(K-Map simplification & Verilog Module)	[10]	2	L3
2		Explain the JK Flip Flop with logic diagram, function table, and equation	[10]	2	L3
3	A	What is Encoder? Write the compressed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position and simplify the same using K-map. Design the logic circuit as well.	[5]	2	L3
	B	What is a Demultiplexer? Design 1:16 Demultiplexer using two 1:8 Demuxes and One 1:2 Demuxes.	[5]		
4	A	With logic diagram and truth table explain the operation of a SR latch	[5]	3	L2
	B	Explain the role of system software in a computing system.	[5]	3	L2
5	A	Explain the single-bus structure with a neat diagram.	[5]	3	L2
	B	Explain Operational Concept of a computer with a diagram.	[5]	3	L2
6	A	What is the difference between Multiplexer and Demultiplexer?	[5]	3	L2
	B	Explain the RISC and CISC instruction types with examples.	[5]	3	L2

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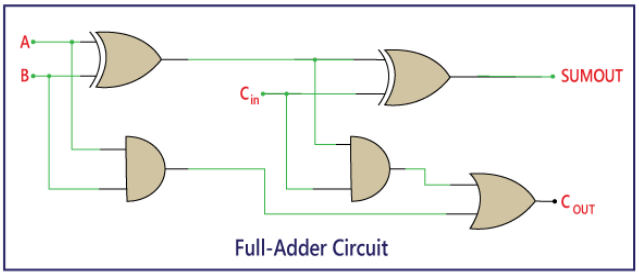
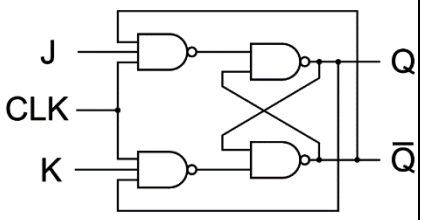
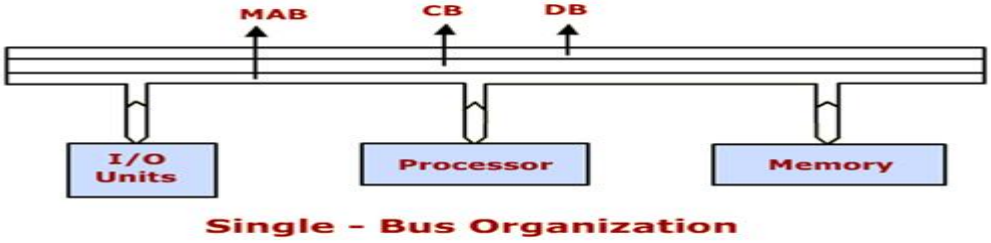
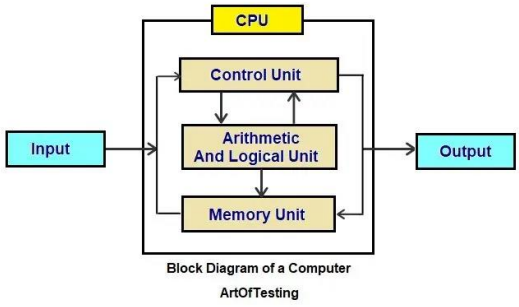
Internal Assessment Test 2 – Jan 2024

Scheme of Valuation

Sub:	Digital Design and Computer Organization					Sub Code:	BCS302 /BAD302	Branch:	AIML/AINI (DS)/CS(AI
Date:	19/12/2023	Duration:	90 minutes	Max Marks:	50	Sem	III		OE

		Answer any FIVE Questions	MARKS	CO
1		Design a full adder by constructing the truth table and simplify the output equations.(K-Map simplification & Verilog Module)  Full-Adder Circuit Inputs / Outputs A B C_{in} Sum Carry 0 0 0 0 0 0 0 1 1 0 0 1 0 1 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 1 Circuit diagram of Full adder Truth Table and K-Map Verilog Code (Any one level)	[10]	1
2		Explain the JK Flip Flop with logic diagram, function table, and equation Circuit Diagram Truth Table Toggle Condition  	[10]	1
3	a	What is Encoder? Write the compressed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position and simplify the same using K-map. Design the logic circuit as well. Encoder Circuit, Truth Table and K-Map for outputs. Expiation for priority assigned to LSB and MSB	[5]	2

	b	What is a Demultiplexer? Design 1:16 Demultiplexer using two 1:8 Demuxes and One 1:2 Demuxes. Circuit Diagram, and connectivity should be shown correctly. Truth table not expected.	5	2
4	a	With logic diagram and truth table explain the operation of a SR latch Either a NOR latch or NAND latch circuit is expected. Truth table when inputs are 0, 0 and 1.1 has to be explained in detail. Memory and Not used conditions.	[5]	3
	b	Explain the role of system software in a computing system. Definition, Their Role and few examples like OS, compiler, Assembler, Linker and Loader Expected.	[5]	3
5	a	Explain the single-bus structure with a neat diagram.  Single – Bus Organization	[5]	3
	b	Explain Operational Concept of a computer with a diagram.  Block Diagram of a Computer ArtOfTesting	[5]	3

6	a	What is the difference between Multiplexer and Demultiplexer?	[5]	3

Parameters	**Multiplexer**	**Demultiplexer**
Definition	Multiplexer refers to a type of combinational circuit that accepts multiple inputs of data but provides only a single output.	The demultiplexer refers to combinational circuit that a single input but directs it th outputs.
Technique of Conversion	A Multiplexer performs conversion from parallel to serial.	A Demultiplexer performs serial to parallel.
Common Name	Data Selector	Data Distributor
Operational Principle	Multiplexer works on an operational principle of *many to one*.	Demultiplexer works on an principle of *one to many*.
Configuration of Devices	It behaves as a data selector because the multiplexer is an N to 1 device.	It behaves as a data distrib demultiplexer is a 1 to N d
Total Number of Data Inputs	It has multiple inputs of data and signals.	It has a single input of data
Total Number of Data Outputs	A Multiplexer generates a single output for data and signals.	A Demultiplexer generates for data and signals.

	b	Explain the RISC and CISC instruction types with examples. ## Characteristics of CISC Processor Following are the main characteristics of the RISC processor: 1. The length of the code is shorts, so it requires very little RAM. 2. CISC or complex instructions may take longer than a single clock cycle to execute the code. 3. Less instruction is needed to write an application. 4. It provides easier programming in assembly language. 5. Support for complex data structure and easy compilation of high-level languages. 6. It is composed of fewer registers and more addressing nodes, typically 5 to 20. 7. Instructions can be larger than a single word. ## Features of RISC Processor Some important features of RISC processors are: 1. **One cycle execution time:** For executing each instruction in a computer, the RISC processors require one CPI (Clock per cycle). And each CPI includes the fetch, decode and execute method applied in computer instruction. 2. **Pipelining technique:** The pipelining technique is used in the RISC processors to execute multiple parts or stages of instructions to perform more efficiently. 3. **A large number of registers:** RISC processors are optimized with multiple registers that can be used to store instruction and quickly respond to the computer and minimize interaction with computer memory. 4. It supports a simple addressing mode and fixed length of instruction for executing the pipeline. 5. It uses LOAD and STORE instruction to access the memory location. 6. Simple and limited instruction reduces the execution time of a process in a RISC.	[5]	3

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