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Internal Assesment Test - 3

Sub:	**Power Electronics**							Code:	**21EE54**
Date:	14.03.2024 12.00 – 1.30PM	Duration:	90 mins	Max Marks:	50	Sem:	V	Branch:	EEE

Answer Any FIVE FULL Questions

	Marks	OBE	
		CO	RBT

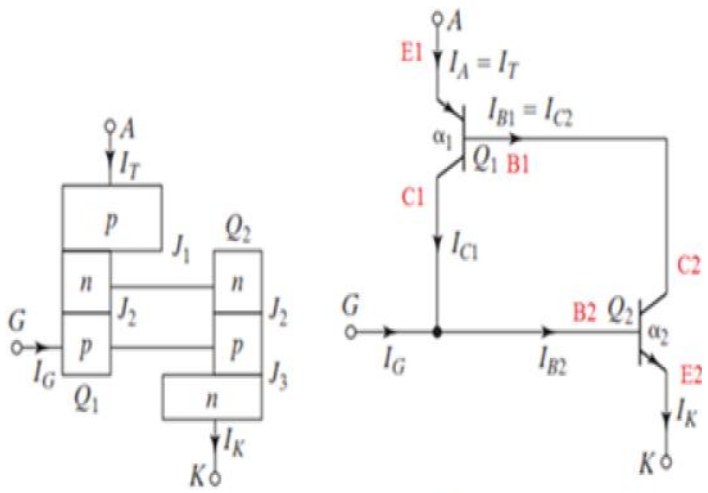
	Explain the two transistor analogy of thyristor, and derive an expression for the anode current of thyristor.	[10]	CO 3	L2

Two-transistor Model of Thyristor

- The regenerative or latching action due to a positive feedback can be demonstrated by using a two-transistor model of thyristor.
- A thyristor can be considered as two complementary transistors
- one *PNP*-transistor,*Q*1, and other *NPN*-transistor, *Q2.*

Two-transistor Model of Thyristor

Two-transistor model of thyristor.



(a) Basic structure (b) Equivalent circuit

Derivation of Anode Current

The collector current I_C of a thyristor is related, in general, to the emitter current I_E and the leakage current of the collector–base junction, I_{CBO}, as

$$I_C = \alpha I_E + I_{CBO} \tag{9.1}$$

and the *common-base current* gain is defined as $\alpha = I_C/I_E$. For transistor Q_1, the emitter current is the anode current I_A, and the collector current I_{C1} can be found from Eq. (9.1):

$$I_{C1} = \alpha_1 I_A + I_{CBO1} \tag{9.2}$$

where α_1 is the current gain and I_{CBO1} is the leakage current for Q_1. Similarly, for transistor Q_2, the collector current I_{C2} is

$$I_{C2} = \alpha_2 I_K + I_{CBO2} \tag{9.3}$$

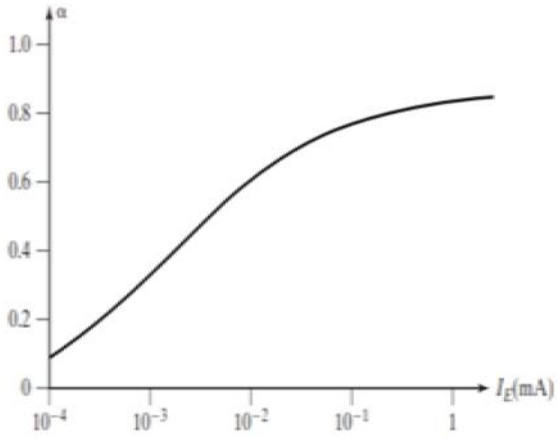
where α_2 is the current gain and I_{CBO2} is the leakage current for Q_2. By combining I_{C1} and I_{C2}, we get

$$I_A = I_{C1} + I_{C2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2} \tag{9.4}$$

For a gating current of I_G, $I_K = I_A + I_G$ and solving Eq. (9.4) for I_A gives

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \tag{9.5}$$

Variation of Current Gain with Emitter Current

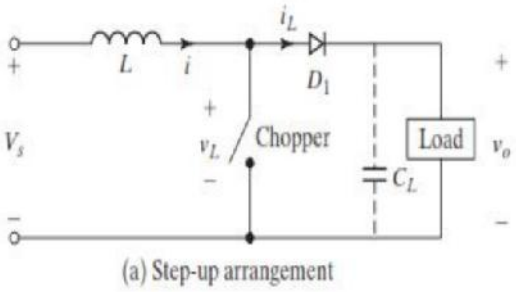


Typical variation of current gain with emitter current.

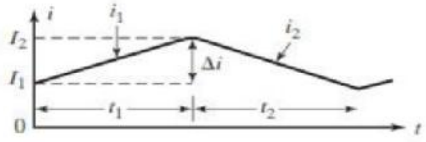
2	**Explain the operation of step-up chopper. Draw the relevant waveform. Derive an expression for average output voltage.** ➢ Step-up chopper is a static device whose average output DC voltage is greater than its input DC voltage. ➢ A converter can be used to step-up a dc voltage and an arrangement for step-up operation. When switch SW is closed for time t, the inductor current rises and energy is stored in the inductor L.	[10]	CO5	L2

- If the switch is opened for time t1, the energy stored in the inductor is transferred to load through diode D and the inductor current falls

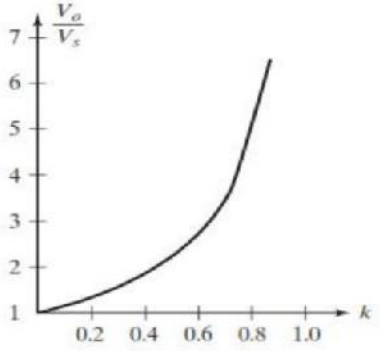
Step-up Chopper



(a) Step-up arrangement

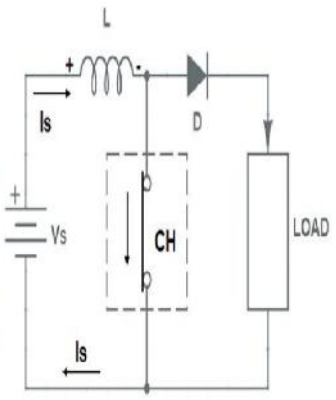


(b) Current waveform



Mode 1: Switch is ON

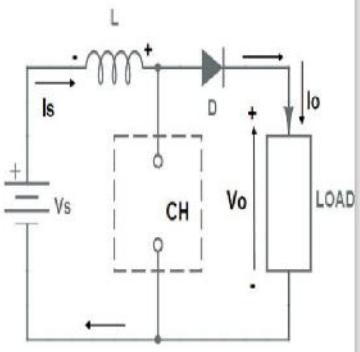
- When chopper (CH) is switched ON, the current will flow through the closed path formed by supply source Vs, inductor L and chopper CH.
- During this period, no current will flow through the load.
- Only source current i_s will flow and the value of load current i_o will be ZERO during the ON period.
- Also, during the T_{ON} period, energy is stored in the inductor L.
- This energy storage in L is essential to boost the load output voltage above the source voltage.
- Therefore, a large value of L is essential in a step-up chopper.



Mode 2: Switch is OFF

- When the chopper CH is switched OFF, the current through the L can not reduce instantaneously rather it decays exponentially.
- Due to this behavior of L, it will force the current through the diode D and load for the entire time period T_{OFF}.
- Since, the current through the inductor L tends to decrease, the polarity of the emf induced in inductor L is reversed as shown in above figure.
- As a result, the voltage across the load becomes equal to the sum of source voltage and emf induced in inductor.
- Thus, the output voltage exceeds the source voltage V_s.
- The load / output voltage may be written as below.

$$V_0 = V_s + L(di/dt)$$



Average Output Voltage Equation

When the converter is turned on, the voltage across the inductor is

$$v_L = L\frac{di}{dt} \Rightarrow di = \frac{v_L}{L}dt = \frac{V_s}{L}t_1$$

and this gives the peak-to-peak ripple current in the inductor as

$$\Delta I = \frac{V_s}{L}t_1$$

The average output voltage is

$$v_o = V_s + L\frac{\Delta I}{t_2}$$

$$= V_s\left(1 + \frac{t_1}{t_2}\right) = V_s\left(1 + \frac{kT}{(1-k)T}\right)$$

$$= V_s\frac{1}{1-k}$$

$$\Delta I = \frac{V_s}{L}t_1$$

$$t_1 = kT$$

$$t_2 = (1-k)T$$

$$v_o = V_s\frac{1}{1-k}$$

K value can be changed from 0 to 1.

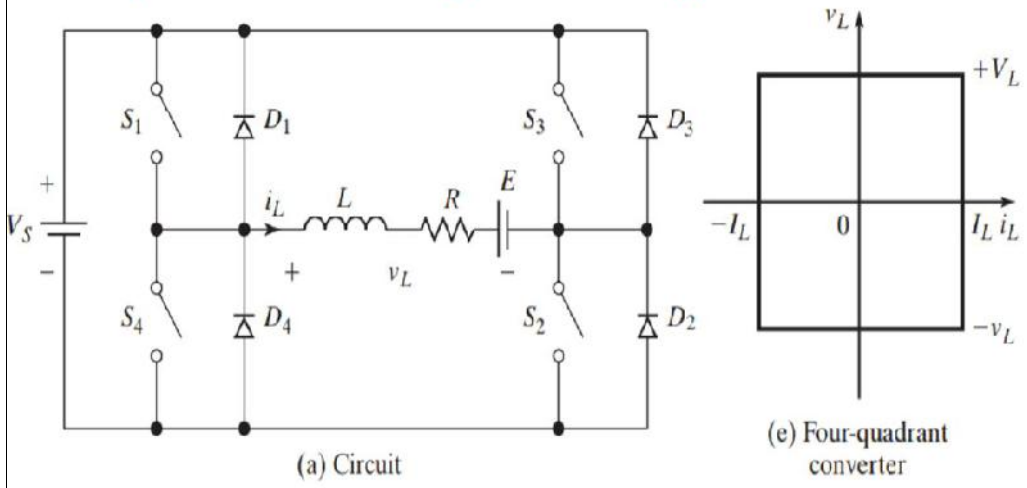
3	Classify the different types of choppers, with the help of circuit and quadrant diagram explain the class E chopper. **Classification of DC-DC Converter / Chopper** DC-DC Converter (Chopper) are classified into five types 1. First quadrant converter / Class A Chopper 2. Second quadrant converter / Class B Chopper	[10]	CO 5	L2

3. First and second quadrant converter / Class C Chopper
4. Third and fourth quadrant converter / Class D Chopper
5. Four-quadrant converter / Class E Chopper

Four-quadrant converter / Class E Chopper

• The load current is either positive or negative
• The load voltage is also either positive or negative.
• One first and second quadrant converter and one third and fourth quadrant converter can be combined to form the four-quadrant converter.
• For operation in the third and fourth quadrant, the direction of the battery E must be reversed.
• This converter forms the basis for the single-phase full-bridge inverter.

Four-quadrant converter / Class E Chopper

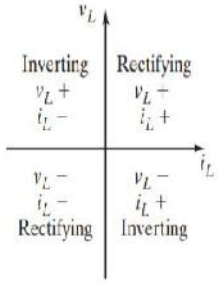


(a) Circuit

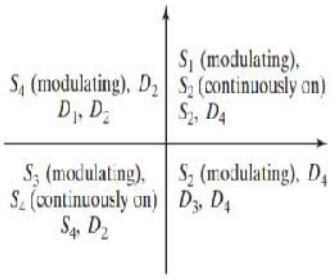
(e) Four-quadrant converter

Four-quadrant Operation

- For an inductive load with an emf (E) such as a dc motor, the four-quadrant converter can control the power flow and motor speed
- Forward motoring (vL positive and iL positive),
- Forward regenerative braking (vL positive and iL negative),
- Reverse Motoring (vL negative and iL negative),
- Reverse regenerative braking (vL negative and iL positive).



(b) Polarities



(c) Conducting devices

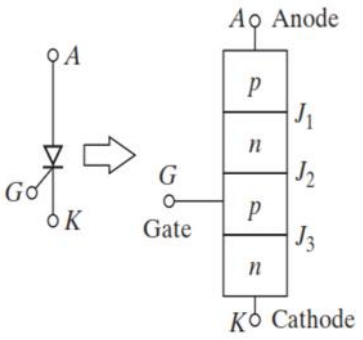
With proper switch control, the four quadrant converter can operate and control flow in any of the four quadrants. For operation in the third and fourth quadrants, the direction of the load emf E must be reversed internally.

4	With neat Graph explain the VI characteristics of thyristor and define latching and holding current.	[10]	CO 3	L2

Thyristor Symbol

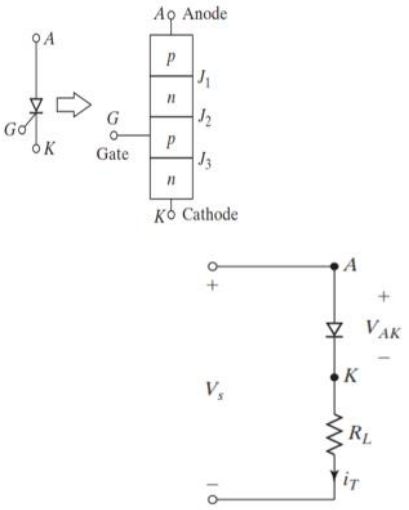
- A thyristor is a
  - ➢ Four-layer semiconductor device of *PNPN* structure
  - ➢ Three *pn*- junctions. J1, J2, J3
  - ➢ It has three terminals:
    - ✓ anode
    - ✓ cathode
    - ✓ gate.
- Thyristors are manufactured by diffusion.

Thyristor symbol and three *pn*-junctions.

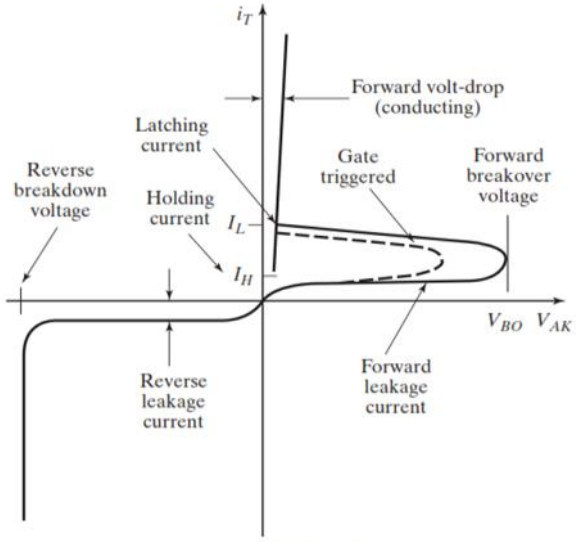


V-I Characteristics of Thyristor

Thyristor symbol and three *pn*-junctions.



(a) Circuit



(b) v–i Characteristics

Thyristor Characteristics

Forward Biased Characteristics

Forward Biased : Anode voltage is positive with respect to Cathode, P layer is connected to positive terminal and N layer is connected to negative layer.

- When the anode voltage is made positive with respect to the cathode, the junctions *J*1 and *J*3 are forward biased.
- The junction J2 is reverse biased, and only a small leakage current flows from anode to cathode.
- The thyristor is then said to be in the *forward blocking*, or *off-state* condition.
- The leakage current is known as *off-state current ID*.

Avalanche Breakdown and Forward Breakdown Voltage

- If the anode-to-cathode voltage *VAK* is increased to a sufficiently large value, the reverse-biased junction *J*2 breaks.
- This is known as *avalanche breakdown* and the corresponding voltage is called *forward breakdown voltage VBO*.
- Because the other junctions *J*1 and *J3* are already forward biased, there is free movement of carriers across all three junctions, resulting in a large forward anode current.
- The device is then in a *conducting state*, or *on-state*.
- The voltage drop would be due to the ohmic drop in the four layers and it is small, typically, 1 V.
- In the on-state, the anode current is limited by an external impedance or a resistance, *RL*.

Thyristor Turn On by Gate Voltage

- A thyristor can be turned on by increasing the forward voltage *VAK beyond VBO*, but such a turn-on could be destructive.
- In practice, the forward voltage is maintained below *VBO* and the thyristor is turned on by applying a positive voltage between its gate and cathode.
- This is shown in Figure by dashed lines.
- Once a thyristor is turned on by a gating signal and its anode current is greater than the holding current, the device continues to conduct due to positive feedback, even if the gating signal is removed.
- A thyristor is a latching device.

Latching Current IL and Holding Current IH

- The anode current must be more than a value known as *latching current IL* to maintain the required amount of carrier flow across the junction; otherwise, the device reverts to the blocking condition as the anode-to-cathode voltage is reduced.
- *Latching current IL* is the minimum anode current required to maintain the thyristor in the on-state immediately after a thyristor has been turned on and the gate signal has been removed.
- Once a thyristor conducts, it behaves like a conducting diode and there is no control over the device.
- The device continues to conduct because there is no depletion layer on the junction *J2* due to free movements of carriers.
- However, if the forward anode current is reduced below a level known as the *holding current IH,* a depletion region develops around junction *J2* due to the reduced number of carriers and the thyristor is in the blocking state.
- The holding current is on the order of milliamperes and is less than the latching current *IL*.
- That is, $IL > IH$
- *Holding current IH* is the minimum anode current to maintain the thyristor in the on-state.
- The holding current is less than the latching current.

Reverse Biased Characteristics:

- **Anode voltage is negative with respect to Cathode, P layer is connected to negative terminal and N layer is connected to positive layer.**
- When the cathode voltage is positive with respect to the anode, the junction *J2* is forward biased but junctions *J1* and *J3* are reverse biased.
- This is like two series-connected diodes with reverse voltage across them.
- The thyristor is in the reverse blocking state and a reverse leakage current, known as *reverse current IR*, flows through the device.

5	a. Explain turn on methods of thyristor.	[5+5]	CO3	L2

Thyristor – Turn ON

- A thyristor is turned on by increasing the anode current.
- This can be accomplished in one of the following ways.

Thermals.

Light.

High voltage.

dv/dt.

Gate current.

Thyristor – Turn ON – By Thermals

- If the temperature of a thyristor is high, there is an increase in the number of electron–hole pairs, which increases the leakage currents.
- This increase in currents causes α1 and α2 to increase.
- Due to the regenerative action, (α1 + α2) may tend to unity and the thyristor may be turned on.

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

- This type of turn-on may cause thermal runaway and is normally avoided.

Thyristor – Turn ON – By Light

- If light is allowed to strike the junctions of a thyristor, the electron–hole pairs increase; and the thyristor may be turned on.
- The light-activated thyristors are turned on by allowing light to strike the silicon wafers.

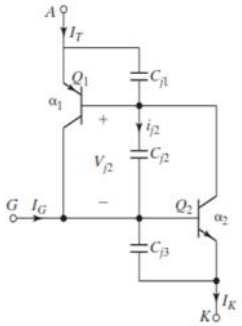
Thyristor – Turn ON – By High Voltage

- If the forward anode-to-cathode voltage VBK is greater than the forward breakdown voltage *VBO*, sufficient leakage current flows to initiate regenerative turn-on.
- This type of turn-on may be destructive and should be avoided.

Thyristor – Turn ON – By dv/dt

If a thyristor is in a blocking state, a rapidly rising voltage applied across the device would cause high current flow through the junction capacitors.

Two-transistor transient model of thyristor.



Current through the capacitor Cj2 is given by

$$i_{j2} = \frac{d(q_{j2})}{dt} = \frac{d}{dt}(C_{j2}V_{j2}) = V_{j2}\frac{dC_{j2}}{dt} + C_{j2}\frac{dV_{j2}}{dt}$$

where C_{j2} and V_{j2} are the capacitance and voltage of junction J_2, respectively, Transistor Q_{j2} is the charge in the junction. If the rate of rise of voltage dv/dt is large, then i_{j2} would be large and this would result in increased leakage currents I_{CBO1} and I_{CBO2}. According to Eq. IA . high enough values of I_{CBO1} and I_{CBO2} may cause $(\alpha_1 + \alpha_2)$ tending to unity and result in undesirable turn-on of the thyristor. However, a large current through the junction capacitors may also damage the device.

Thyristor – Turn ON – By dv/dt

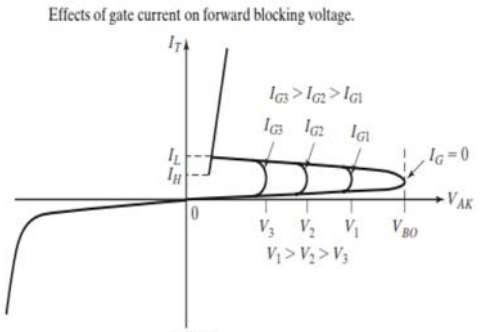
Current through the capacitor Cj2 is given by

$$i_{j2} = \frac{d(q_{j2})}{dt} = \frac{d}{dt}(C_{j2}V_{j2}) = V_{j2}\frac{dC_{j2}}{dt} + C_{j2}\frac{dV_{j2}}{dt}$$

- If the rate of rise of the anode– cathode voltage is high, the charging current of the capacitive junctions may be sufficient enough to turn on the thyristor.
- A high value of charging current may damage the thyristor; and the device must be protected against high *dv/dt*.
- The manufacturers specify the maximum allowable *dv/dt* of thyristors.

Thyristor – Turn ON – By Gate Current

- If a thyristor is forward biased, the injection of gate current by applying positive gate voltage between the gate and cathode terminals turns on the thyristor.
- As the gate current is increased, the forward blocking voltage is decreased.



b. Explain UJT firing circuit for the SCR.

Unijunction Transistor (UJT)

What is Unijunction Transistor (UJT)

- UJT stands for **U**ni**J**unction **T**ransistor.
- It is a three terminal semiconductor switching device.
- The Unijunction Transistor is a simple device that consists of a bar of n-type silicon material with a non-rectifying contact at either end (base 1 and base 2), and with a rectifying contact (emitter) alloyed into the bar part way along its length, to form the only junction within the device (hence the name 'Unijunction').
- The Unijunction Transistor is also known as Double Base Diode.

Symbol and Construction of Unijunction Transistor (UJT)

In Unijunction Transistor, the PN Junction is formed by lightly doped N type silicon bar with heavily doped P type material on one side. The ohmic contact on either ends of the silicon bar is termed as Base 1 (B_1) and Base 2 (B_2) and P-type terminal is named as emitter.

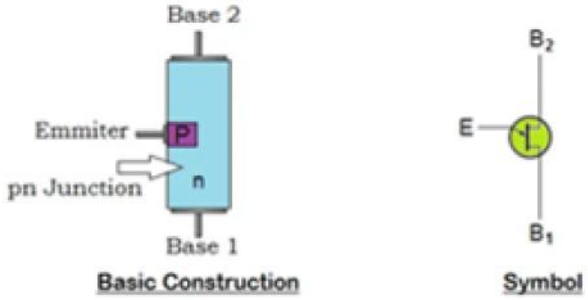
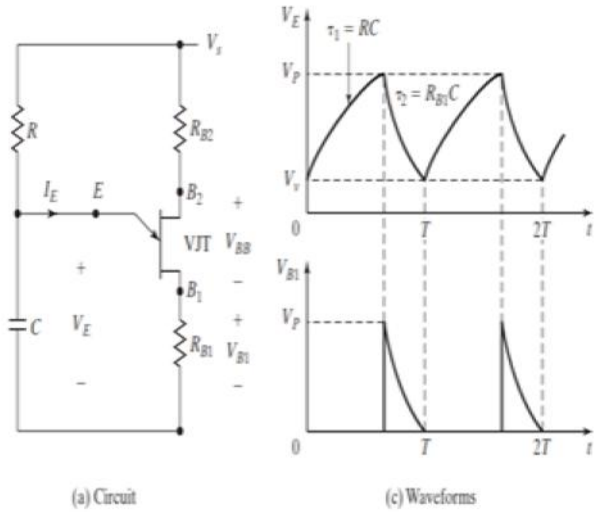


Fig. 2 – Basic Construction & Symbol of Unijunction Transistor (UJT)

The emitter junction is placed such that it is more close to terminal Base 2 than Base 1. The symbols of both UJT and JFET resemble the same except the emitter arrowhead represents the direction in which conventional current flow, but they operate differently.

UJT Circuit, Waveforms,



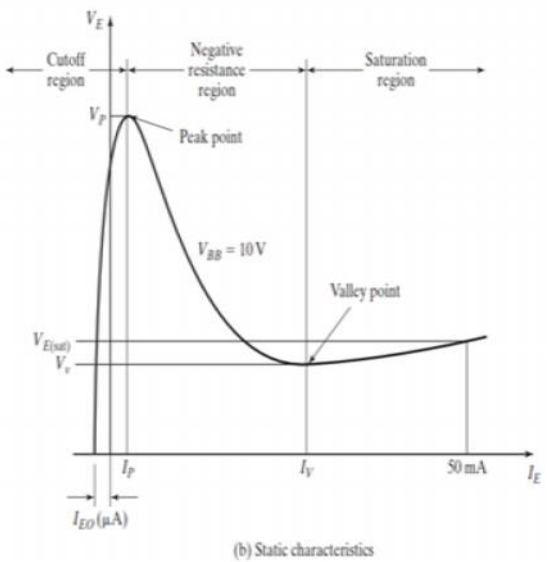
(a) Circuit (c) Waveforms

The static characteristics of a UJT

- When the dc supply voltage *Vs* is applied, the capacitor *C is charged through Resistor* because the emitter circuit of the UJT is in the open state.
- The time constant of the charging circuit is $\tau 1 = RC$.
- When the emitter voltage *VE*, which is same as capacitor voltage vc, reaches the *peak voltage Vp*, the UJT turns on and capacitor *C* discharges through *RB*1 at a rate determined by the time constant $\tau 2 = R_{B1}C$ is much smaller than $\tau 1$.
- When the emitter voltage *VE* decays to the valley point *Vv*, the UJT turns off, and the charging cycle is repeated.
- The waveform of the triggering voltage *VB1* is identical to the discharging current of capacitor *C*. The triggering voltage *VB*1 should be designed to be sufficiently large to turn on the SCR.
- The period of oscillation, *T*, is fairly independent of the dc supply voltage *Vs.*

- **Peak-Point Emitter Current. I_p**. It is the emitter current at the peak point. It repre-sents the minimum current that is required to trigger the device (UJT). It is inversely proportional to the interbase voltage V_{BB}.
- **Valley Point Voltage V_V** The valley point voltage is the emitter voltage at the valley point. The valley voltage increases with the increase in interbase voltage V_{BB}.
- **Valley Point Current I_V** The valley point current is the emitter current at the valley point. It increases with the increase in inter-base voltage V_{BB}.
- **Special Features of UJT.** The special features of a UJT are :
- A stable triggering voltage (V_P)— a fixed fraction of applied inter base voltage V_{BB}.
- A very low value of triggering current.
- A high pulse current capability.
- A negative resistance characteristic.
- Low cost.

UJT Static Characteristics



(b) Static characteristics

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- Cutoff region Cutoff region is the area where the Unijunction Transistor (UJT) doesn't get sufficient voltage to turn on. The applied voltage VE hasn't reached the triggering point, thus making transistor to remain in off state.
- Negative Resistance region When the emitter reaches the triggering voltage, VTRIG, Unijunction Transistor (UJT) will turn on. After a certain time, if the voltage applied to the emitter lead increases, it will reach out at VPEAK. The voltage drops from VPEAK to Valley Point even though the current increases (negative resistance).
- Saturation region is the part of characteristic curve in which the current and voltage both increase, if the applied voltage to emitter terminal increases.

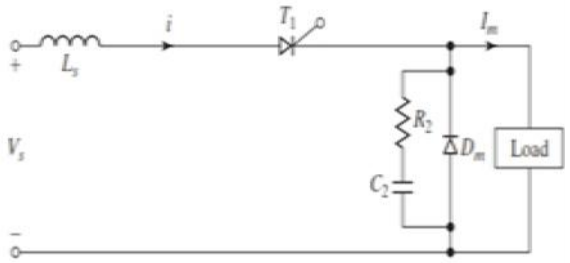
6	a. Explain the di/dt protection of thyristor.	[5+5]	CO3	L2 L3

Q6. a. Describe how thyristors are protected from di/dt. (6 marks)

di/dt Protection

- A thyristor requires a minimum time to spread the current conduction uniformly throughout the junctions.
- If the rate of rise of anode current is very fast compared with the spreading velocity of a turn-on process, a localized "hot-spot" heating may occur due to high current density and the device may fail, as a result of excessive temperature.
- The practical devices must be protected against high *di/dt.*
- Under steady-state operation, *Dm* conducts when thyristor *T*1 is off.
- If *T*1 is fired when *Dm* is still conducting, *di/dt* can be very high and limited only by the stray inductance of the circuit.
- **In practice, the *di/dt* is limited by adding a series inductor *Ls***

di/dt Protection with Limiting Inductor Ls



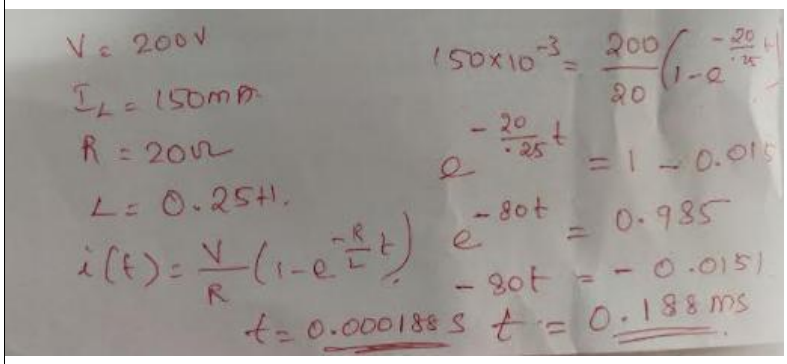
Thyristor switching circuit with *di/dt* limiting inductors.

The forward *di/dt* is

$$\frac{di}{dt} = \frac{V_s}{L_s}$$

where L_s is the series inductance, including any stray inductance.

b.A thyristor operating at 200V, latching current is 150mA, for a load of 20ohms and 0.25H, find the minimum width of gate pulse required to turn on the thyristor.



7	Explain the voltage control techniques of single-phase Inverter.	[10]	CO5	L2

Voltage Control of single-phase Inverters

- In many industrial applications, the control of the output voltage of inverters is often necessary

(1) to cope with the variations of dc input voltage,

(2) to regulate voltage of inverters,

(3) to satisfy the constant voltage and frequency control requirement.

- There are various techniques to vary the inverter gain.
- The most efficient method of controlling the gain (and output voltage) is to incorporate PWM control within the inverters.

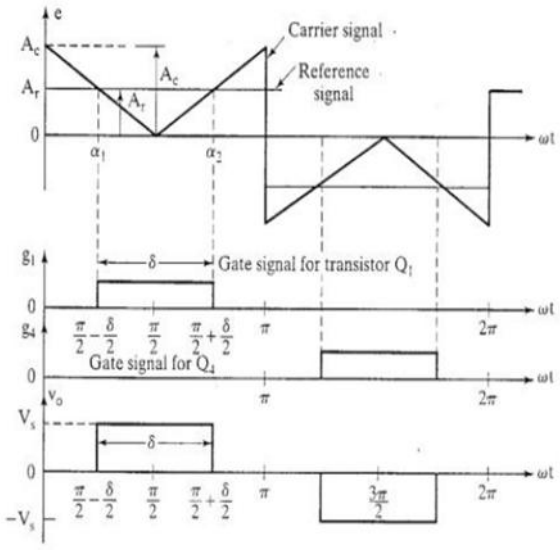
PWM Control Techniques

1. Single-pulse-width modulation
2. Multiple-pulse-width modulation
3. Sinusoidal pulse-width modulation
4. Modified sinusoidal pulse-widthmodulation
5. Phase-displacement control

✓The constant DC input voltage is applied at the input of the inverter and output voltage controlled by switching semiconductor device of the inverter in this method.

- Among all these techniques, the sinusoidal pulse-width modulation (SPWM) commonly used for a voltage control.
- However, the multiple-pulse-width modulation provides a foundation for bett understanding of the PWM modulation techniques.
- The modified SPWM gives limited ac output voltage control.
- The phase-displacement control is normally used for high-voltage applicatior especially phase displacement by transformer connections.

1. Single-pulse-width modulation



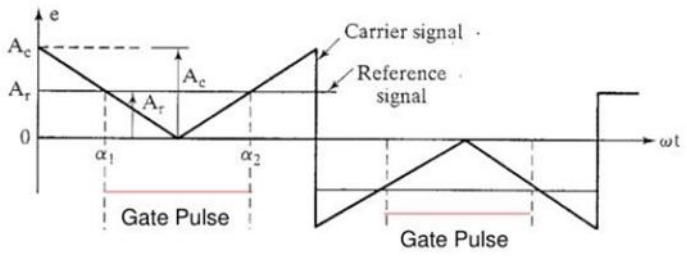
Output Voltage Vo = Vs (g1- g4)

Single-pulse-width modulation

- In single-pulse width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the inverter output voltage.
- The gating signals are generated by comparing a rectangular reference signal of amplitude, Ar, with a triangular carrier wave of amplitude Ac.
- The fundamental frequency of output voltage is determined by the frequency of the reference signal.
- The pulse-width, δ, can be varied from 0° to 180° by varying Ar from 0 to Ac.
- The ratio of Ar to Ac is the control variable and is defined as the amplitude modulation index.
- The amplitude modulation index, or simply modulation index is

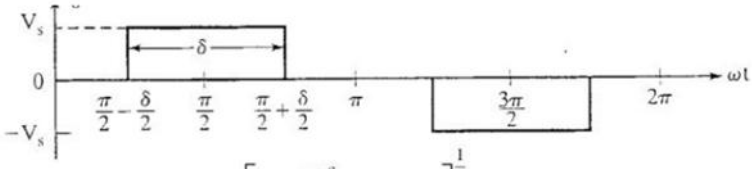
$$\text{Modulation Index} = M = A_r/A_c$$

Modulation Index



- Compare the Reference Signal with the Carrier
- Frequency of the Reference Signal determines the frequency of the Output Voltage
- Modulation Index = M = A_r/A_c

RMS Output Voltage



$$V_o = \left[\frac{2}{2\pi}\int_{\frac{\pi-\delta}{2}}^{\frac{\pi+\delta}{2}} V_s^2\, d(\omega t)\right]^{\frac{1}{2}}$$

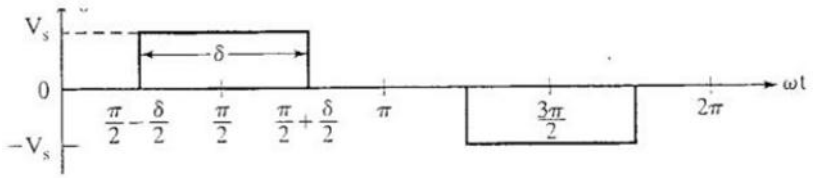
$$V_o = V_s\sqrt{\frac{\delta}{\pi}}$$

$$0° \le \delta \le 180°$$

$$0 \le V_o \le V_s$$

The pulse-width, δ, (0° to 180°) by varying Ar from 0 to Ac, Vo can be varied from 0 to Vs

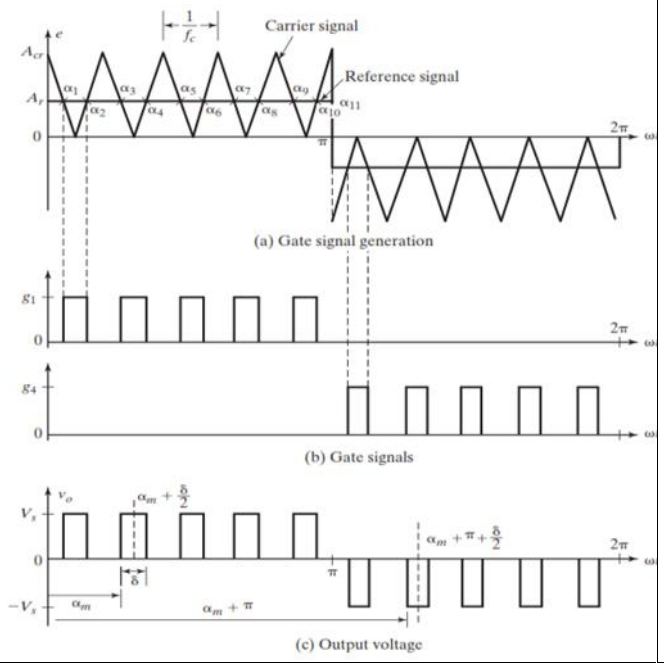
Fourier Series of the Output Voltage



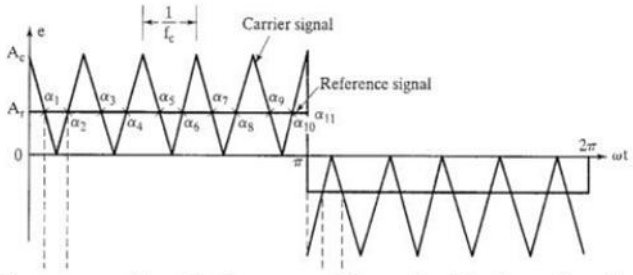
$$v_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin\frac{n\delta}{2} \sin n\omega t$$

2. Multi Pulse Width Modulation

Output Voltage Vo = Vs (g1- g4)



Gate Signal Generation



- Compare the Reference Signal with the Carrier
- Frequency of the Reference Signal determines the Output Voltage Frequency
- Frequency of the Carrier determines the number of pulses per half-cycle
- Modulation Index controls the Output Voltage

Frequency Modulation Ratio

- The frequency of reference signal sets the output frequency *fo*
- the carrier frequency *fc* determines the number of pulses per half-cycle *p*.
- The modulation index controls the output voltage.
- This type of modulation is also known as *uniform pulse-width modulation* (UPWM).
- The number of pulses per half-cycle is found from

$$P = \frac{f_c}{2f_o} = \frac{m_f}{2}$$

- Where mf is the frequency modulation ratio
- mf = fc / fo

RMS Output Voltage

If δ is the width of each pulse, the rms output voltage can be found from

$$V_o = \left[\frac{2p}{2\pi}\int_{(\pi/p-\delta)/2}^{(\pi/p+\delta)/2} V_s^2\, d(\omega t)\right]^{1/2} = V_s\sqrt{\frac{p\delta}{\pi}}$$

$$V_o = V_s\sqrt{\frac{p\delta}{\pi}}$$

The variation of the modulation index $M = A_r/A_{cr}$ from 0 to 1 varies the pulse width δ from 0 to $T/2p$ (0 to π/p) and the rms output voltage V_o from 0 to V_s.

$$0 \le M \le 1 \qquad 0 \le \delta \le \frac{T}{2p} \qquad 0 \le \delta \le \frac{\pi}{p} \qquad 0 \le V_o \le V_s$$

Features of Multi pulse width modulation

- The order of harmonics is the same as that of single-pulse modulation.
- The distortion factor is reduced significantly compared with that of single-pulse modulation.
- However, due to larger number of switching on and off processes of power transistors, the switching losses would increase.
- With larger values of *p*, the amplitudes of LOH would be lower, but the amplitudes of some higher order harmonics would increase.
- However, such higher order harmonics produce negligible ripple or can easily be filtered out.

Sinusoidal Pulse Width Modulation

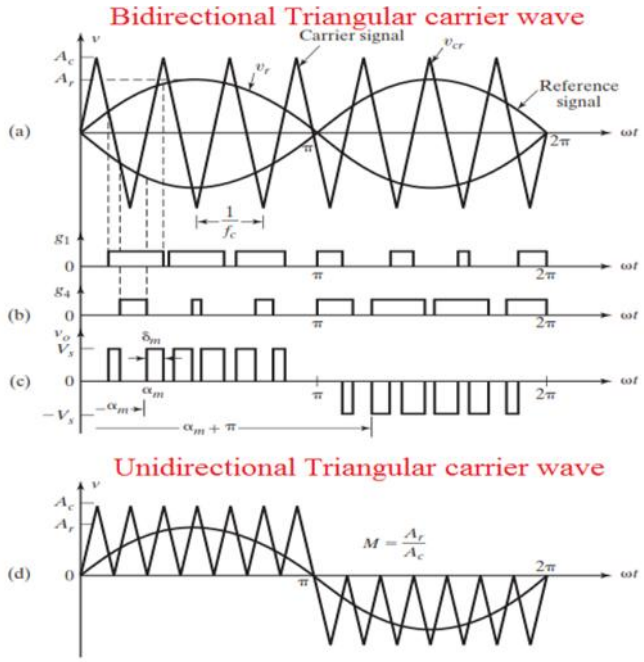
- Since the desired output voltage is a sine wave, a reference sinusoidal signal is used as the reference signal.
- Instead of maintaining the width of all pulses the same as in the case of multiple-pulse modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse.
- The DF and LOH are reduced significantly.
- The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency *fc.*
- This sinusoidal pulse-width modulation (SPWM) is commonly used in industrial applications.
- The frequency of reference signal *fr* determines the inverter output frequency *fo*; and its peak amplitude *Ar,* controls the modulation index *M, then controls RMS output voltage.*

Sinusoidal Pulse Width Modulation

✓Comparing the bidirectional carrier signal v*cr* with two sinusoidal reference signals v*r* and -vr shown in produces gating signals *g*1 and *g*4, respectively.

✓Unidirectional triangular wave if preferred

Output Voltage Vo = Vs (g1- g4)



RMS Output Voltage

The rms output voltage can be varied by varying the modulation index M, defined by $M = A_r/A_c$.

If δ_m is the width of mth pulse

the rms output voltage by summing the average areas under each pulse as

$$V_o = V_s\left(\sum_{m=1}^{2p}\frac{\delta_m}{\pi}\right)^{1/2}$$

The peak fundamental output voltage for PWM and SPWM control can be found approximately from

$$V_{m1} = dV_s \quad \text{for } 0 \le d \le 1.0$$

d > 1, Over modulation

Fourier series of the output voltage

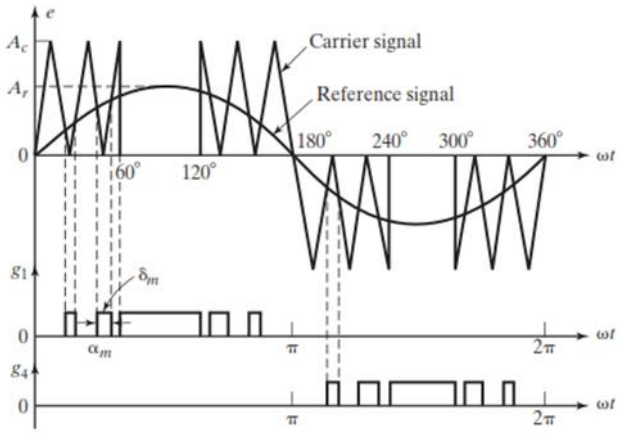
$$v_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} B_n \sin n\omega t$$

$$B_n = \sum_{m=1}^{2p}\frac{4V_s}{n\pi}\sin\frac{n\delta_m}{2}\left[\sin n\left(\alpha_m + \frac{\delta_m}{2}\right)\right] \quad \text{for } n = 1, 3, 5, \ldots$$

✓ The DF is significantly reduced compared with that of multiple-pulse modulation.

✓ This type of modulation eliminates all harmonics less than or equal to $2p - 1$. For $p = 5$, the LOH is ninth.

Modified sinusoidal pulse-Width modulation



Modified sinusoidal pulse-Width modulation

- SPWM technique can be modified so that the carrier wave is applied during the first and last 60° intervals per half-cycle (e.g., 0° to 60° and 120° to 180°).
- The fundamental component is increased and harmonic characteristics are improved.
- It reduces the number of switching of power devices and reduces the switching losses.

No of pulses and frequency ratio

The number of pulses q in the 60° period is normally related to the frequency ratio, particularly in three-phase inverters, by

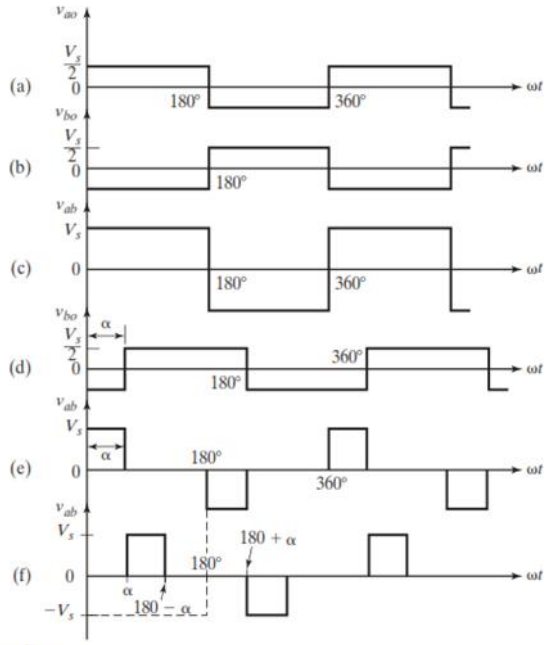
$$\frac{f_c}{f_o} = 6q + 3$$

The instantaneous output voltage is $v_o = V_s(g_1 - g_4)$. The algorithm for generating the gating signals is similar to that for sinusoidal PWM except the reference signal is a sine wave from 60° to 120° only.

5. Phase Displacement Control

- Voltage control can be obtained by using multiple inverters and summing the out-put voltages of individual inverters.
- A single-phase full-bridge inverter can be perceived as the sum of two half-bridge inverters.

Phase Displacement Control



RMS and Instantaneous Output Voltage

The rms output voltage,

$$V_o = V_s\sqrt{\frac{\alpha}{\pi}} \tag{6.44}$$

If $V_{ao} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin n\omega t$

$$v_{bo} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin n(\omega t - \alpha)$$

The instantaneous output voltage,

$$v_{ab} = v_{ao} - v_{bo} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi}[\sin n\omega t - \sin n(\omega t - \alpha)]$$

which, after using $\sin A - \sin B = 2\sin[(A - B)/2]\cos[(A + B)/2]$, can be simplified to

$$v_{ab} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin \frac{n\alpha}{2} \cos n\left(\omega t - \frac{\alpha}{2}\right) \tag{6.45}$$

The rms value of the fundamental output voltage is

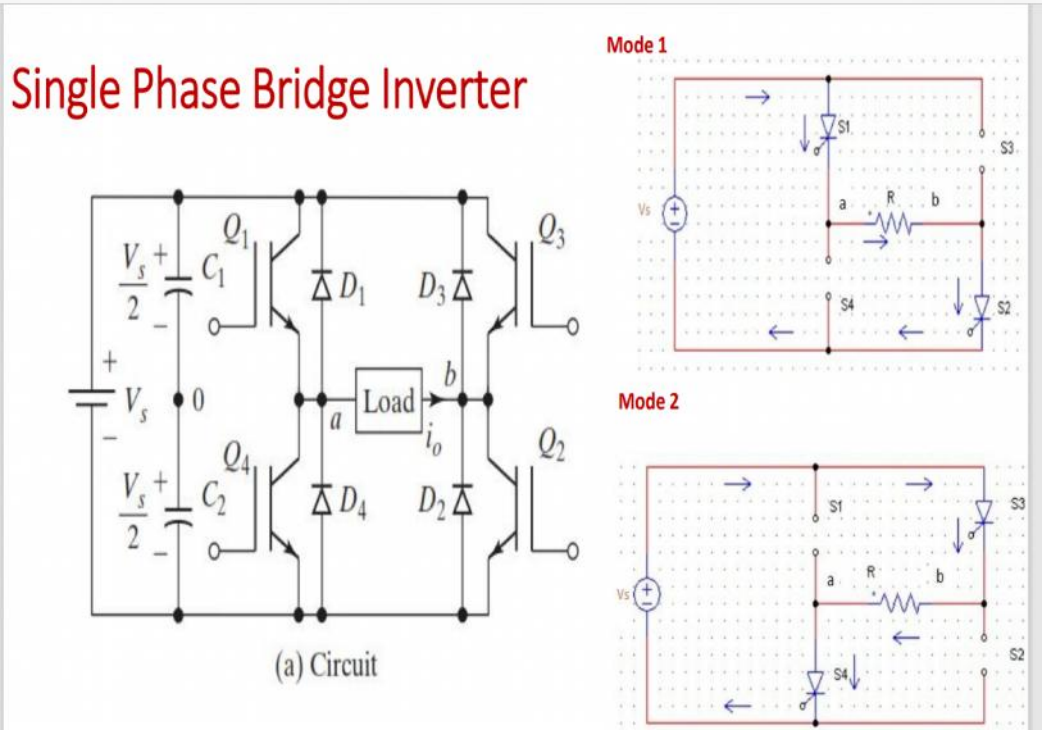
$$V_{o1} = \frac{4V_s}{\pi\sqrt{2}} \sin \frac{\alpha}{2} \tag{6.46}$$

Equation (6.46) indicates that the output voltage can be varied by changing the delay angle. This type of control is especially useful for high-power applications, requiring a large number of switching devices in parallel.

8	**With the neat circuit diagram and waveforms, Explain the operation of single-phase full bridge inverter supplying resistive a load.**	[10]	CO5	L2

Single Phase Bridge Inverter

- Full bridge single phase inverter is a switching device that generates a square wave AC output voltage on the application of DC input by adjusting the switch turning ON and OFF based on the appropriate switching sequence, where the output voltage generated is of the form +Vs, -Vs, Or 0.
- A single-phase bridge voltage-source inverter (VSI)
- It consists of four choppers (Q1 D1, Q2 D2, Q3 D3, Q4 D4).
- When transistors *Q*1 and *Q2* are turned on simultaneously, the input voltage *Vs* appears across the load.
- If transistors *Q*3 and *Q4* are turned on at the same time, the voltage across the load is reversed and is -*Vs*.

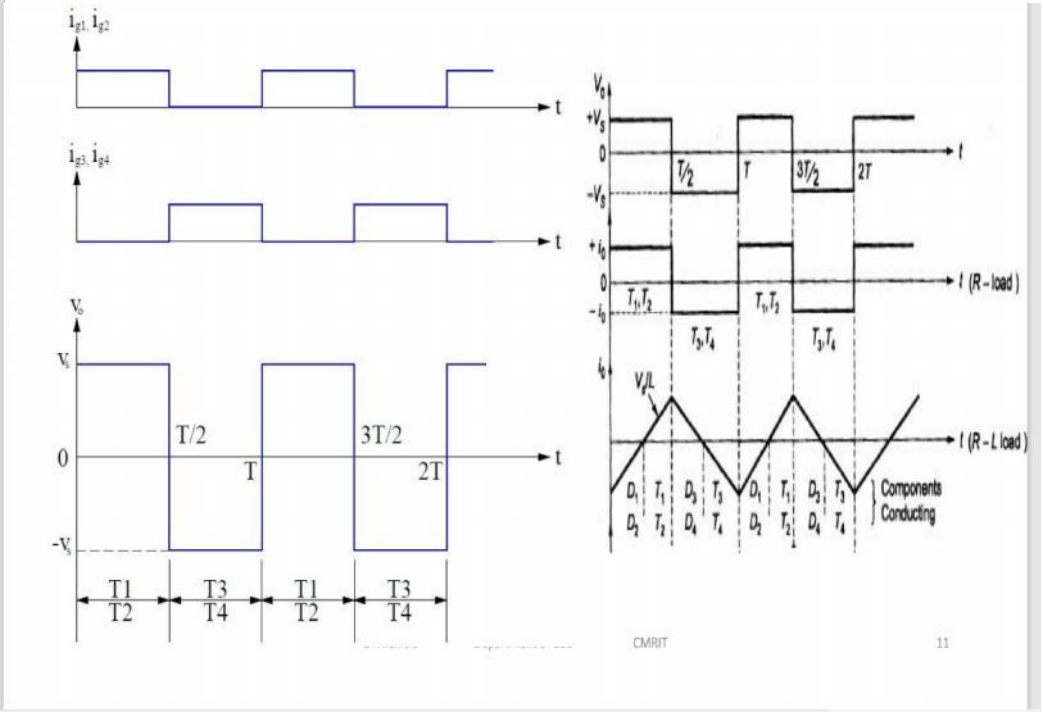


Mode 1 (0 to T/2):-

- During this mode switch S1 and switch S2 are ON and switch S3 and switch S4 are OFF From period 0 to T/2.
- Current flowing path during this mode is Vs – S1- a -R(load reistor) – b – S2 – Vs.
- Voltage across the load resistor is positive Vs. (Vo = Vs)

Mode 2 (T/2 to T):-

- During this mode switch S3 and switch S4 are ON and switch S1 and switch S2 are OFF From period T/2 to T.
- Current flowing path during this mode is Vs – S3 – b – R(load resistor) – a – S4 – Vs.
- Voltage across the load resistor is negative Vs. (Vo = -Vs)



Switching States of single phase full bridge inverter

Switch States for a Single-Phase Full-Bridge Voltage-Source Inverter

State	State No.	Switch State*	v_{ao}	v_{bo}	v_o	Components Conducting
S_1 and S_2 are on and S_4 and S_3 are off	1	10	$V_S/2$	$-V_S/2$	V_S	S_1 and S_2 if $i_o > 0$ D_1 and D_2 if $i_o < 0$
S_4 and S_3 are on and S_1 and S_2 are off	2	01	$-V_S/2$	$V_S/2$	$-V_S$	D_4 and D_3 if $i_o > 0$ S_4 and S_3 if $i_o < 0$
S_1 and S_3 are on and S_4 and S_2 are off	3	11	$V_S/2$	$V_S/2$	0	S_1 and D_3 if $i_o > 0$ D_1 and S_3 if $i_o < 0$
S_4 and S_2 are on and S_1 and S_3 are off	4	00	$-V_S/2$	$-V_S/2$	0	D_4 and S_2 if $i_o > 0$ S_4 and D_2 if $i_o < 0$
S_1, S_2, S_3, and S_4 are all off	5	off	$-V_S/2$ $V_S/2$	$V_S/2$ $-V_S/2$	$-V_S$ V_S	D_4 and D_3 if $i_o > 0$ D_1 and D_2 if $i_o < 0$

designed such that Q_1 and Q_2 are not turned on at the same time. Figure b shows the waveforms for the output voltage and transistor currents with a resistive load. It should be noted that the phase shift is $\theta_1 = 0$ for a resistive load. This inverter requires a three-wire dc source, and when a transistor is off, its reverse voltage is V_s instead of $V_s/2$. This inverter is known as a *half-bridge inverter.*

The root-mean-square (rms) output voltage can be found from

$$V_o = \left(\frac{2}{T_0} \int_0^{T_0/2} \frac{V_s^2}{4} dt \right)^{1/2} = \frac{V_s}{2}$$

The instantaneous output voltage can be expressed in Fourier series as

$$v_o = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t))$$

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Internal Assesment Test - 3

Sub:	**Power Electronics**							Code:	**21EE54**
Date:	14.03.2024 12.00 – 1.30PM	Duration:	90 mins	Max Marks:	50	Sem:	V	Branch:	EEE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Explain the two transistor analogy of thyristor, and derive an expression for the anode current of thyristor.	[10]	CO3	L2
2	Explain the working of step-up chopper with a neat circuit and waveform and derive the average and RMS output voltage.	[10]	CO5	L2
3	Classify the different types of choppers, with the help of circuit and quadrant diagram explain the class E chopper.	[10]	CO5	L2
4	With neat Graph explain the VI characteristics of thyristor and define latching and holding current.	[10]	CO3	L3

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5	a. Explain turn on methods of thyristor. b. Explain UJT firing circuit for the SCR.	[5+5]	CO3	L4
6	a. Explain the di/dt protection of thyristor. b. A thyristor operating at 200V, latching current is 150mA, for a load of 20ohms and 0.25H, find the minimum width of gate pulse required to turn on the thyristor.	[5+5]	CO3	L2 L3
7	Explain the voltage control techniques of single-phase Inverter.	[10]	CO5	L2
8	With neat circuit and waveform explain the single phase full bridge inverter.	[10]	CO5	L2

CI **CCI** **HOD**

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