USN | | | | | | | | | |

18CS34

Third Semester B.E. Degree Examination, June/July 2024
Computer Organization

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a.   With a neat diagram, analyze the basic operational concept of a computer. Give the operational steps (operational steps). **(10 Marks)**

    b.   What is performance measurement? Explain the overall SPEC rating for the computer in a program suite. **(10 Marks)**

OR

2   a.   Define addressing mode, explain the various addressing mode with examples. **(10 Marks)**

    b.   Explain in detail, various shift and rotate instruction and example with neat diagram. **(10 Marks)**

Module-2

3   a.   With neat diagram, explain various methods for handling multiple interrupts requests raised by multiple devices. **(10 Marks)**

    b.   What is DMA Bus Arbitration? Briefly explain different bus arbitration techniques. **(10 Marks)**

OR

4   a.   What is an interrupt? What are interrupt service routine and what are vector interrupts? Explain with example. **(10 Marks)**

    b.   Explain the following with respect to USB:
    i)   U.S.B. Architecture
    ii) U.S.B. protocols. **(10 Marks)**

Module-3

5   a.   Draw a diagram and explain the working of 16 megabit DRAM chip configured as $2m \times 8$. **(10 Marks)**

    b.   Explain direct mapping technique and associative mapping technique in mapping function. **(10 Marks)**

OR

6   a.   Analyze how data are written into (ROM) Read Only Memory. Discuss different types of Read Only Memories. **(10 Marks)**

    b.   What is cache memory? Explain any two mapping functions of cache memory. **(10 Marks)**

Module-4

7   a.   Convert the following pairs of decimal numbers to 5-bit signed 2's complement binary numbers and add them. State whether or not over flow occurs in each case:
    i)   5 and 10
    ii) -14 and 11
    iii) -5 and 7
    iv) -10 and -13 **(04 Marks)**

b. Design the 16 bit carry look ahead adder using 4-bit adder. Also write the expression for C_{i+1}. **(10 Marks)**

c. Draw the two n-bit number x and y to perform addition/subtraction. **(06 Marks)**

OR

8 a. With an example explain the Booths algorithm to multiply two signed operands. **(10 Marks)**

b. Multiply each of the following pairs of signed 2's complement number using the booth algorithm (A = multiplicand and B = multiplier)
   i)   A = 010111 and B = 110110
   ii) A = 110011 and B = 101100
   iii) A = 110101 and B = 011011
   iv) A = 001111 and B = 001111 **(10 Marks)**

Module-5

9 a. Discuss with neat diagram, the single bus organization of the data path inside a processor. **(10 Marks)**

b. Write the sequence of control steps required for single bus structure for each if the following instructions.
   i) Add the contents of memory location NUM to register R1.
   ii) Add the contents of memory location whose address is at memory location NUM to register R1. **(10 Marks)**

OR

10 a. Explain the following:
   i) Hard-wired control
   ii) Microprogrammed control. **(10 Marks)**

b. What is pipeline? Explain the 4 stages pipeline with its instruction execution steps and hardware organization. **(10 Marks)**

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