CBCS SCHEME

USN | | | | | | | | | | |

17CS72

Seventh Semester B.E. Degree Examination, June/July 2024
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With the help of block diagrams, explain Flynn's classification of computer architectures. **(10 Marks)**

b. Describe the shared-memory multiprocessor models. **(10 Marks)**

OR

2 a. Define the types of data dependence. Also compute the dependence graph for the following code segment:

S_1 : Load R1, A
S_2 : Add R2, R1
S_3 : Move R1, R3
S_4 : Store B, R1 **(10 Marks)**

b. Explain the characteristics of the following static connection networks :
(i) Linear array. (ii) Ring. (iii) Binary tree. (iv) Mesh. **(10 Marks)**

Module-2

3 a. Explain the architecture of VLIW processor and its pipeline operations. **(08 Marks)**

b. Distinguish between typical RISC and CISC processor architectures. **(06 Marks)**

c. With a neat diagram, explain the hierarchical memory technology. **(06 Marks)**

OR

4 a. Explain Inclusion, Coherence and Locality properties. **(06 Marks)**

b. Briefly explain the virtual memory models for multiprocessor system. **(06 Marks)**

c. With a diagram, explain a typical superscalar RISC processor architecture consisting of an integer unit and a floating point unit. **(08 Marks)**

Module-3

5 a. Illustrate daisy-chained and distributed arbitration techniques. **(10 Marks)**

b. List the various Cache mapping schemes. Also explain any two schemes. **(10 Marks)**

OR

6 a. Consider the following pipeline reservation table:

Time →

Stages	1	2	3	4	5	6	7
S_1	X						X
S_2		X		X			
S_3			X		X		

(i) What are the forbidden latencies?
(ii) What is the initial collision vector?
(iii) Draw the state transition diagram
(iv) List all the simple cycles.
(v) List all the greedy cycles.
(vi) Determine the minimal average Latency. **(10 Marks)**

b. Explain the usage of prefetch buffers in instruction pipelining. **(06 Marks)**

c. Illustrate internal data forwarding technique. **(04 Marks)**

Module-4

7 a. Explain briefly different vector access memory schemes. **(06 Marks)**

b. Explain four context switching policies. **(08 Marks)**

c. Explain routing in Omega network. **(06 Marks)**

OR

8 a. Explain Snoopy protocols, with its approaches. **(10 Marks)**

b. With a diagram, explain the architecture of the connection machine CM - 2. **(10 Marks)**

Module-5

9 a. Define Parallel Programming Model. Explain shared and distributed parallel models. **(08 Marks)**

b. Explain Concurrent OOP and Actor model in Object Oriented Parallel Programming Model. **(05 Marks)**

c. Explain principles of Synchronization in Parallel Programming in Multiprocessing. **(07 Marks)**

CMRIT LIBRARY
BANGALORE - 560 037

OR

10 a. With the help of neat diagram, explain Computation phases in code generation in parallel computation. **(07 Marks)**

b. Explain different language features of Parallel programming. **(08 Marks)**

c. Write a note on Dependency Testing. Briefly. **(05 Marks)**

* * * * *

VTU-20-06-2024 01:08:15pm - CR - CR - CR