Seventh Semester B.E. Degree Examination, June/July 2024
Advanced Computer Architecture

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1   a.   Define computer architecture. Illustrate the seven dimensions of an ISA.   **(08 Marks)**
    b.   What is dependability? Explain two main measures of dependability.   **(06 Marks)**
    c.   A compiler designer is trying to describe between two code sequence for a particular high level language statement. Consider two code sequences that require the following instruction counts.

Code sequence	Instruction counts for Instruction class		
	A	B	C
1	2	1	2
2	4	1	1

      (i)   Which code sequence executes of the instruction?
      (ii)   What is the CPI for each sequence?
      (iii)   Which will be faster?   **(06 Marks)**

2   a.   Enlist the pipeline hazards. Also explain them.   **(10 Marks)**
    b.   With an aid of a neat functional diagram, discuss the classic 5 – stage pipeline for a Risc processor, that highlight how an instruction flows through the data path.   **(10 Marks)**

3   a.   Explain in detail 3 different types of dependency.   **(10 Marks)**
    b.   Discuss the methods used to reduce branch costs with prediction.   **(10 Marks)**

4   a.   Explain the issues in implementing advanced speculation.   **(09 Marks)**
    b.   Explain with neat diagram Pentium 4 pipeline supporting multiple issues with speculation.   **(08 Marks)**
    c.   Write note on Branch target buffer.   **(03 Marks)**

PART – B

5   a.   Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential?   **(06 Marks)**
    b.   Discuss the directory – based cache coherence protocol in a distributed memory multiprocessor, indicating the state transition diagram explicitly.   **(07 Marks)**
    c.   What do you understand by memory consistently? Explain furthermore, discuss how relaxed consistently models allow reads and write to complete out of order.   **(07 Marks)**

6   a.   Explain the four memory hierarchy questions in detail.   **(08 Marks)**
    b.   Discuss 3C's of cache miss.   **(04 Marks)**
    c.   Discuss about the methods used to reduce miss penalty.   **(08 Marks)**

7   a. Which are the major categories of advanced optimization of cache performance? Explain any two.   **(10 Marks)**

      b. Explain internal organization of 64 kB DRAM with a diagram.   **(05 Marks)**

      c. Write a note on virtual machine.   **(05 Marks)**

8   a. Discuss how software pipelining and trance scheduling techniques are useful in uncovering the parallelism among instructions by creating longer sequences of straight sine code.   **(10 Marks)**

      b. Explain the five different execution unit types in the IA-64 architecture, that hold the corresponding instruction classes.   **(10 Marks)**

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