CBCS SCHEME

USN | | | | | | | | | |

18EC34

Third Semester B.E. Degree Examination, June/July 2024
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Design a combinational logic circuit so that an output is generated indicating when a majority of four inputs is true. **(06 Marks)**

b. Place the following equations into the proper canonical form
i) $f(w, x, y, z) = \overline{w}x + y\overline{z}$ ii) $f(A, B, C, D) = A + \overline{B} + C)(\overline{A} + D)$ **(06 Marks)**

c. Using K-map determine minimal sum of product expressions and implement the simplified equation using only NAND gates $f(w, x, y, z) = \Sigma m(1, 2, 3, 4, 9) + \Sigma d\ (10, 11, 12, 13, 14, 15)$ **(08 Marks)**

OR

2 a. Define the following terms literal, canonical sum of products, Karnaugh Map, Prime implicatns. **(04 Marks)**

b. Find the minimal sum of the following Boolean function using Quine McClusky method $f(w, x, y, z) = \Sigma(1, 3, 13, 15) + \Sigma d(8, 9, 10, 11)$ **(08 Marks)**

c. Using K-map determine minimal product of sum expression and implement the simplified equation using only NOR gates $f(a, b, c, d) = \pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$. **(08 Marks)**

Module-2

3 a. Implement following multiple output function using 74LS138 decoder
$F_1(A, B, C) = \Sigma m(1, 4, 5, 7)$
$F_2(A, B, C) = \pi m(2, 3, 6, 7)$ **(06 Marks)**

b. Explain 4-bit carry look ahead adder with necessary diagram and relevant expression. **(10 Marks)**

c. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$ using 8 : 1 MUX with a, b, c as select lines **(04 Marks)**

OR

4 a. Implement full adder using 74138 decoder. **(06 Marks)**

b. Design a 2-bit Magnitude comparator. **(08 Marks)**

c. Design 4-line to 2 line priority uncoder which gives MSB the highest priority and LSB least priority. **(06 Marks)**

Module-3

5 a. What is race around condition? Explain JK master slave flip-flop with diagram function table and timing diagram. **(08 Marks)**

b. Explain the working of 4-bit Johnson counter using necessary diagram and waveform. **(06 Marks)**

c. Explain with a neat diagram and truth table, a 4-bit SIPO shift register to store binary number 1010. **(06 Marks)**

OR

6 a. Explain the operation of switch debouncer using SR latch with the help of circuit and waveform. **(06 Marks)**

b. Explain the working of 3-bit Asynchronous up-down counter with necessary waveform and truth table. **(10 Marks)**

c. Write the difference between combinational circuits and sequential circuits. **(04 Marks)**

Module-4

7 a. Design a synchronous Mod -6 counter using clocked D- Flip-Flop. **(10 Marks)**

b. Design a Moore type sequence detector to detect a serial input sequence of 101. **(10 Marks)**

OR

8 a. Construct the excitation table, transition table and state diagram for the sequential circuit shown in Fig Q8(a).

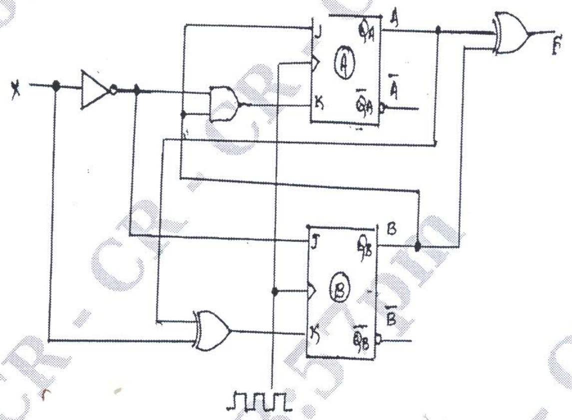

Fig Q8(a) **(10 Marks)**

b. Design a synchronous decade counter using T-flip flop and draw the logic diagram. **(10 Marks)**

Module-5

9 a. List the guidelines for construction of state graphs. **(10 Marks)**

b. Design a sequential circuit to convert BCD to excess – 3 code with state table state graph and transition table. **(10 Marks)**

OR

10 a. Explain with block diagram design of serial Adder with accumulator. **(10 Marks)**

b. Explain with block diagram design of Binary multiplier. **(10 Marks)**

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