(10 Marks)

(10 Marks)

Time hrs

hird Semester B.E. Degree Examination, June/July 2024

Computer Organization and Architecture

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

	Module-1							
1	a.	Explain the operation of a computer with neat block diagram.	(10 Marks)					
	b.	Explain system software functions in detail.	(05 Marks)					
	c.	Explain bus structures.	(05 Marks)					
		OR						
2	a.	Define byte addressability, Big-endian and Little-endian assignment	(06 Marks)					
	b.	Explain following registers:						
	0.	i) PC ii) IR iii) MAR.	(06 Marks)					
	c.	Explain basic performance equation.	(08 Marks)					
		Module-2						
3	a.	List and explain the generic addressing modes with assembler syntax and	addressing					
3	u.	function.	(10 Marks)					
	b.	What are assembler directives? Explain any five assembler directives.	(10 Marks)					
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		OR						
4	a.	Explain stack concepts with diagram.	(08 Marks)					
	b.	Explain shift and rotate operations with examples.	(06 Marks)					
	C.	List the steps involved in 'CALL' and 'RETURN' instructions.	(06 Marks)					
		B- Dr C.F						
		Module-3						
5	a.	Explain memory mapped I/O access.	(10 Marks)					
J	b.	What is an interrupt? With an example explain the concept of interrupt.	(10 Marks)					
		OR						
6	a.	Explain Daisy chain method used for handling simultaneous interrupt request.	(08 Marks)					
U	b.	Explain the use of DMA controller in computer system.	(06 Marks)					
	c.	Explain the concept of vectored interrupt.	(06 Marks)					

Module-4

Explain the internal organization of $2M \times 8$ dynamic memory chip.

Explain virtual memory organization.

OR

8 a. Explain secondary storage device. b. Explain acche memory and its relevant terms. c. Explain different types of non volatile memory. Module-5 9 a. Discuss the single bus organization of data path inside a processor. b. Draw and explain multiple bus organization of CPU. 10 a. Explain block diagram of a complete processor. b. Explain micro programmed control concept. c. Discuss the organization of hardwired controlled unit. 10 a. Explain with the control concept. b. Discuss the organization of hardwired controlled unit. 10 a. Explain with the control concept. b. Explain with the control concept. c. Discuss the organization of hardwired controlled unit. 10 a. Explain block diagram of a complete processor. b. Explain with the control concept. c. Discuss the organization of hardwired controlled unit. 10 a. Explain block diagram of a complete processor. b. Explain block diagram of a complete processor. c. (10 Marks) 10 a. Explain block diagram of a complete processor. b. Explain block diagram of a complete processor. c. (10 Marks) 11 a. Explain block diagram of a complete processor. c. (10 Marks) 12 a. Explain block diagram of a complete processor. c. (10 Marks) 12 a. Explain block diagram of a complete processor. c. (10 Marks) 13 a. Explain block diagram of a complete processor. c. (10 Marks) 14 a. Explain block diagram of a complete processor. c. (10 Marks) 15 a. Explain block diagram of a complete processor. c. (10 Marks) 16 b. Explain block diagram of a complete processor. c. (10 Marks) 17 a. Explain block diagram of a complete processor. c. (10 Marks) 18 a. Explain block diagram of a complete processor. c. (10 Marks) 10 a. Explain block diagram of a complete processor. c. (10 Marks) 10 a. Explain block diagram of a complete processor. c. (10 Marks)			UK	(00 3/4 1)
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