



## Third Semester B.E. Degree Examination, June/July 2024 Electronic Devices

Max. Marks: 100

**Note:** Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. With neat diagrams, explain the different types of bonding forces in solids. (06 Marks)
- b. Write explanatory notes on Intrinsic material with respect to electron hole pairs creation, generation rate and recombination rate. (06 Marks)
- c. With a neat diagram, explain Hall effect and Hall voltage with necessary equations. Explain how Hall effect can be used to detect whether a given unknown sample of semi-conductor is p-type of n-type. (08 Marks)

OR

- 2 a. Explain the energy band structure of solids for insulator, semi-conductor and metal with neat diagram. (04 Marks)
- b. With neat energy band diagrams and chemical bond model of dopants, explain the formation of n-type and p-type semi-conductors. (08 Marks)
- c. Derive the expression for drift velocity of electrons with applied electric field. (08 Marks)

### Module-2

- 3 a. With neat diagram, explain the effect of Forward bias of a p-n junction, with respect to transition width, electric field, electrostatic potential barrier, energy band diagram and particle flow and current direction within transition region 'W'. (08 Marks)
- b. Explain Zener Breakdown with neat energy band diagram. Explain the significance of impact ionization in Avalanche Breakdown with neat diagrams. Derive the expression for Electron multiplication factor  $M_n$ . (08 Marks)
- c. Draw the Piecewise-Linear approximations of a junction diode and explain how a diode can be used as rectifier. (04 Marks)

OR

- 4 a. What are Photodiodes? Explain the significance of current in an illuminated junction and derive the equation for photodiode current and open circuit voltage  $V_{OC}$ . (09 Marks)
- b. What are the necessary requirements to utilize maximum amount of optical energy to design a solar cell, with neat diagrams. (05 Marks)
- c. Explain the principle of operation of Light Emitting Diode (LED) with necessary biasing and requirement of energy band gap energy. (06 Marks)

### Module-3

- 5 a. With neat diagrams of normal biasing and I-V characteristics, explain the working of a p-n-p transistor. (06 Marks)
- b. Derive the expression for ' $\alpha$ ' and ' $\beta$ ' of a transistor in terms of base transport factor 'B' and emitter injection efficiency ' $\gamma$ '. (06 Marks)
- c. Starting from the current component of emitter current  $I_{EN}$  collects current  $I_{CN}$  in normal mode and  $I_{EI}$  and  $I_{CI}$  in inverted mode with hole concentrations  $\Delta_{PE}$  and  $\Delta_{PC}$ , derive the Ebers Moll equations. (08 Marks)



OR

- 6 a. With a neat equivalent circuit diagram, explain the coupled-diode property of Ebers Moll equations. (08 Marks)
- b. With a neat switching circuit of BJT in common-emitter configuration, explain the switching operation. (08 Marks)
- c. With a neat waveform of collector current during transient define the terms delay time ( $t_d$ ), rise time ( $t_r$ ) and fall time  $t_f$ . (04 Marks)

**Module-4**

- 7 a. With neat cross sectional diagrams, I-V characteristics and zero gate voltage, explain the effect of drain voltage on drain current. (06 Marks)
- b. With a neat diagram, explain the small signal equivalent circuit of JFET, Arriving at ideal small-signal equivalent circuit derive the expression for the drain current  $I_{ds}$ . (08 Marks)
- c. What are the two frequency limitation factors in a JFET? With small signal equivalent circuit with capacitance, derive the expression for cutoff frequency  $f_T$ . (06 Marks)

OR

- 8 a. With a cross section diagrams and circuit symbols, explain the operation of  
i) a n-channel enhancement mode MOSFET (06 Marks)  
ii) a n-channel depletion mode MOSFET.
- b. Explain the energy band diagrams of the MOS capacitor with a n-type substrate for various Gate biases. (06 Marks)
- c. With neat cross section diagram and  $I_D$  versus  $V_{DS}$  curve when  $V_{GS} > V_T$ , explain the operation of the MOS structure for :  
i) a small  $V_{DS}$     ii) a larger  $V_{DS}$     iii)  $V_{DS} = V_{DS(sat)}$     iv)  $V_{DS} > V_{DS(sat)}$ . (08 Marks)

**Module-5**

- 9 a. With a neat Schematic diagram, explain Rapid Thermal Processing. (06 Marks)
- b. Explain about Ion implantation with a neat Schematic diagram. (08 Marks)
- c. With a neat diagram, explain Low Chemical Vapor Deposition (LPCVD). (06 Marks)

OR

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- 10 a. Discuss the advantages of Integration of circuits. (08 Marks)
- b. With a neat diagram of simplified description to steps describe the fabrication of p-n diodes on a wafer. (08 Marks)
- c. Describe the types of Integrated circuits. (04 Marks)

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