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CMR INSTITUTE OF TECHNOLOGY

Internal Assesment Test – I									
Sub:	**VLSI DESIGN & TESTING**							**Code:**	**21EC63**
Date:	**04.06.2024**	**Duration:**	**90 mins**	**Max Marks:**	**50**	**Sem**	**VI**	**Branch**	**ECE-A,B,C,D**

Answer Any Five Questions

	Questions	Marks	OBE	
			CO	RBT
1.	Explain the operation of an n-channel enhancement mode MOSFET with neat diagrams.	[10]	CO1	L1
2.	Derive the expression for drain to source current for an n-channel MOSFET in all three regions.	[10]	CO1	L2
3.	Describe in detail about any five non-ideal I-V characteristics of MOS transistor.	[10]	CO1	L2

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4.	Realize the following logic expression using CMOS: a) $Y = A + \overline{BC}$ b) $Y = \overline{(A + B + C).D}$	[10]	CO1	L2
5.	Design a 4:1 multiplexer using transmission gate.	[10]	CO1	L2
6.	Illustrate with neat sketch, explain the DC transfer characteristics of CMOS inverter (Include the condition for all five regions).	[10]	CO1	L2

CI **CCI** **HOD**

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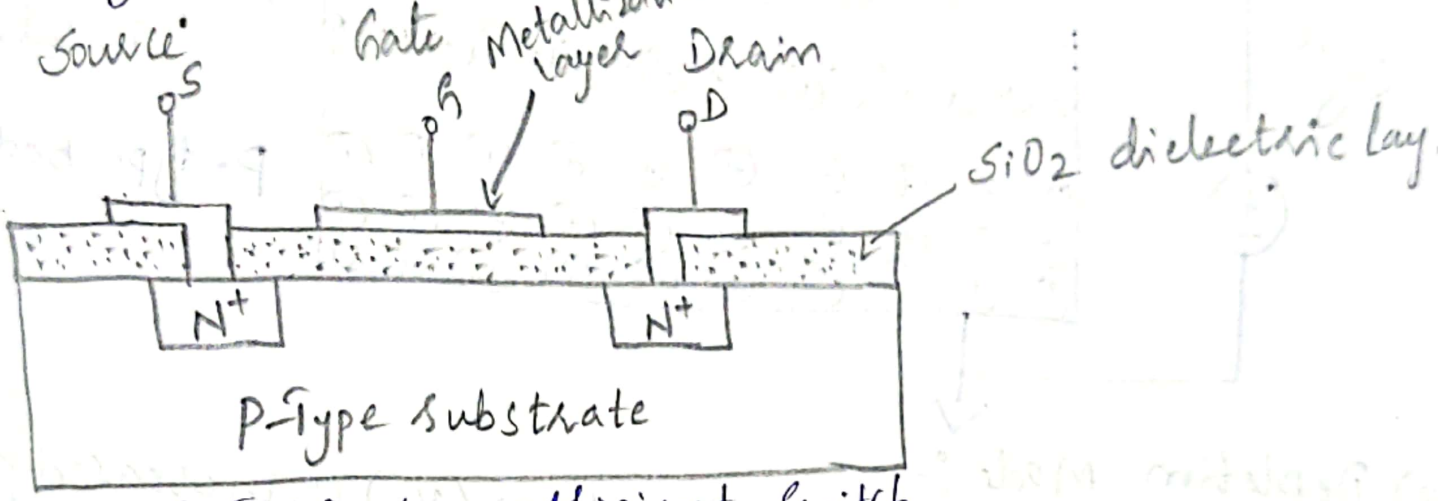
CI **CCI** **HOD**

1. Explain the operation of an n-channel enhancement mode MOSFET with neat diagrams.

a. The transistors consists of 'sandwich' of P-Substrate material, insulating layer and metal layers.

b. The source and drain are created by diffusing two n^+ regions on p-type silicon.

c. The region b/w source and drain is called channel.



d. The MOSFET is very efficient switch.

e. The switch is normally open in enhancement MOSFET.

f. When no positive voltage is applied b/w source and drai (Vds) to gate voltage $\boxed{V_{gs} = 0V}$ then least one of the PN junction is reverse biased.

g. There is no current flow in the substrate and region under the gate, the MOSFET is in OFF condition.

h. At this condition, if the gate voltage is increased then the gate changes from p-type to n-type.

i. The minimum voltage that should be applied to gate is calle 'Threshold voltage – V_t'

j. Based on the applied voltage on V_{gs}, there are three modes of operations are as follows:

(a) Accumulation Mode

(b) Depletion Mode

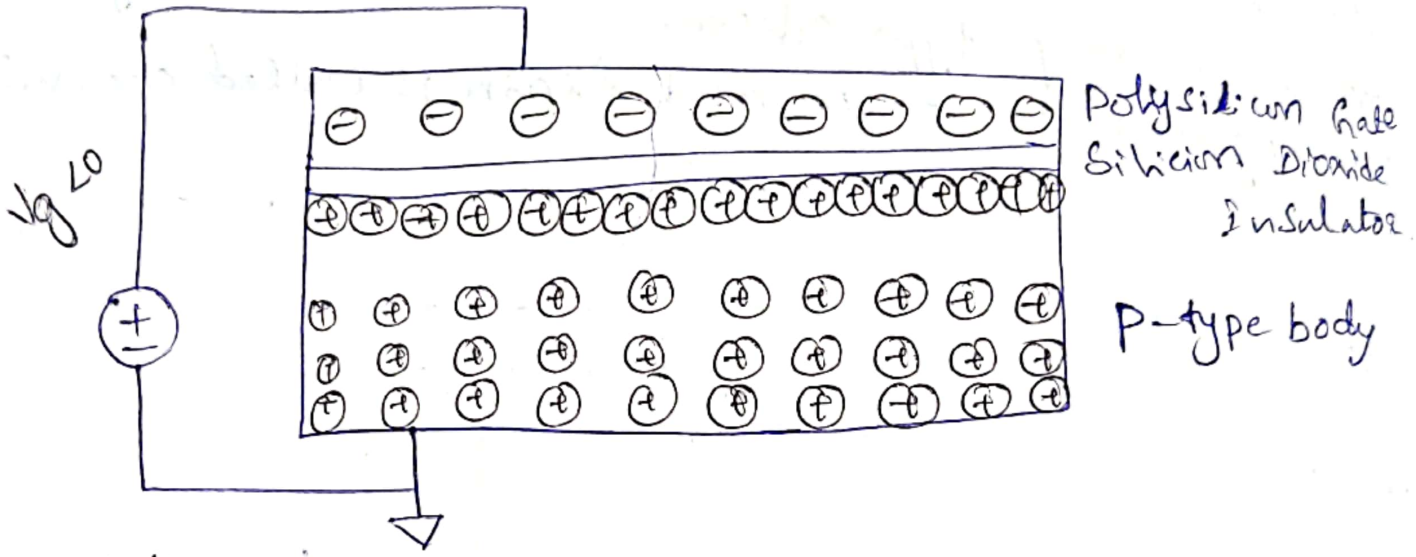
(c) Inversion Mode.

(a) Accumulation Mode :-

(i) When the gate voltage is zero (0) much lower than V_t then it is known as accumulation mode.

(ii) In this mode there is no conduction b/w source and drain.

(iii) The device is in off condition.

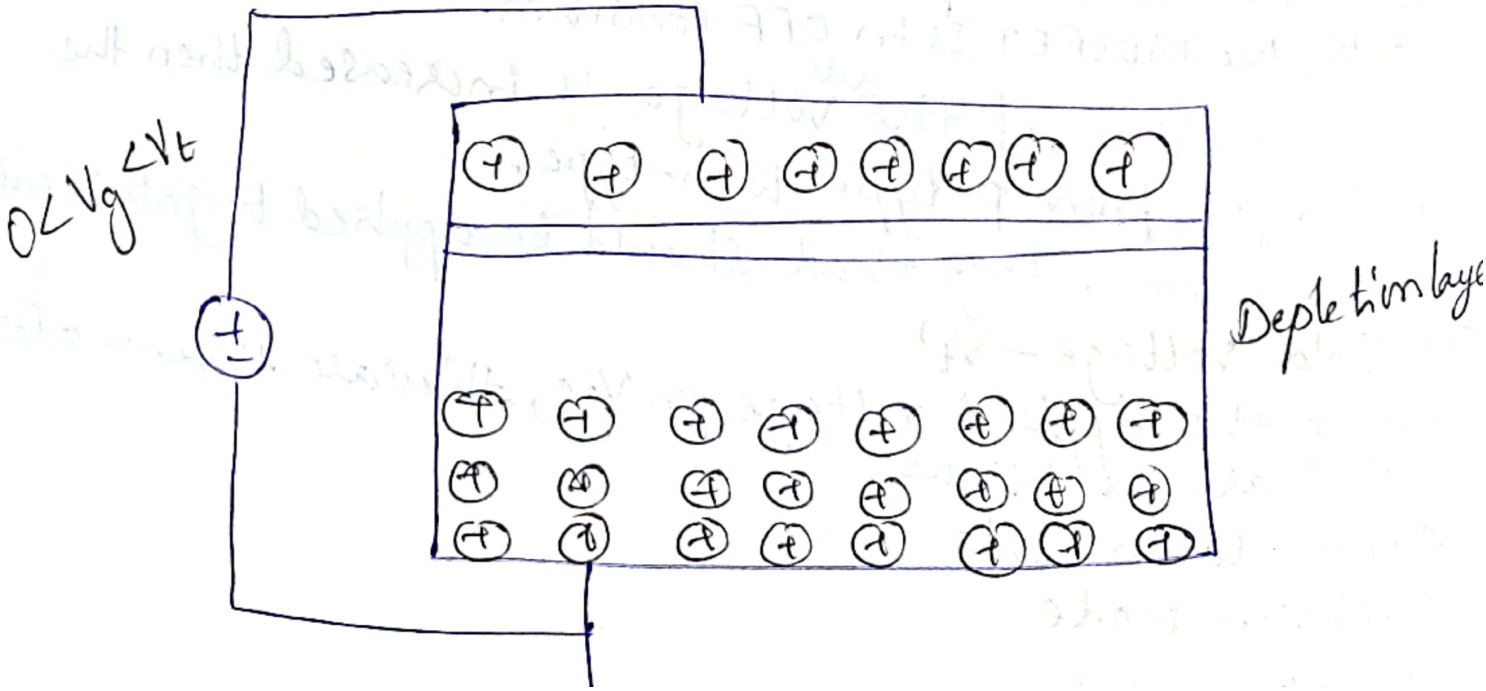


(b) Depletion Mode :-

(i) When the gate to source voltage (V_{gs}) is increased greater than threshold voltage (V_t) the electrons are attracted towards the gate.

(ii) The holes are repelled which forms a depletion region under the gate.

(iii) This structure is called depletion mode.

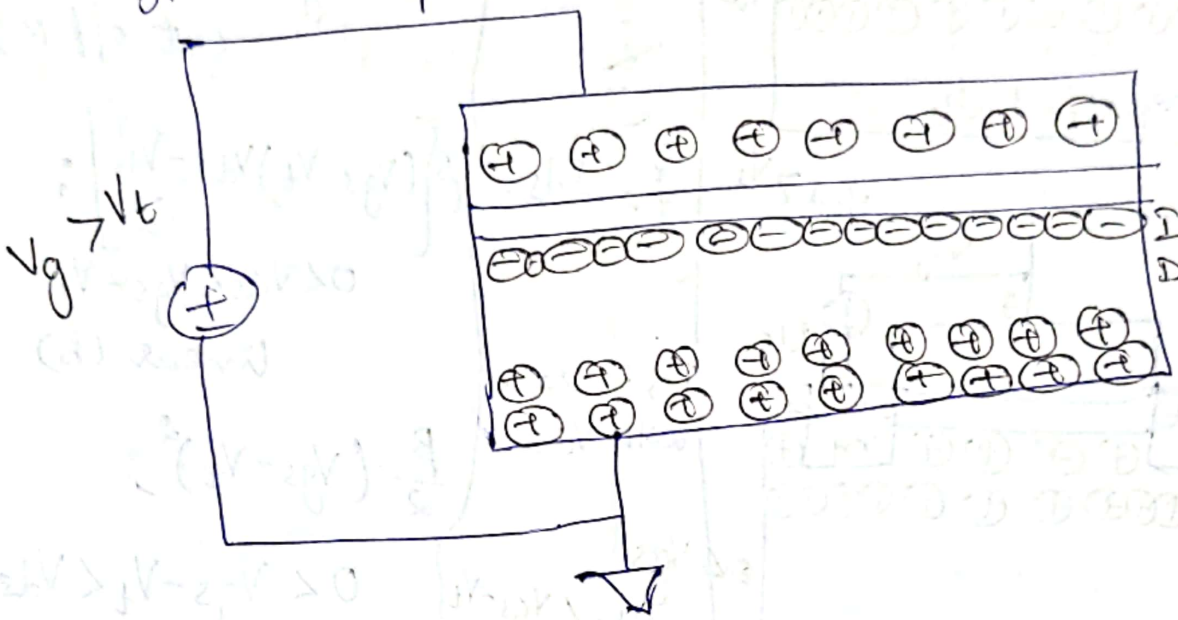


(c) Inversion Mode:

(i) When the gate to source voltage is raised above V_t, the electrons are attracted towards the substrate.

(ii) And the holes are repelled towards the regim under the gate.

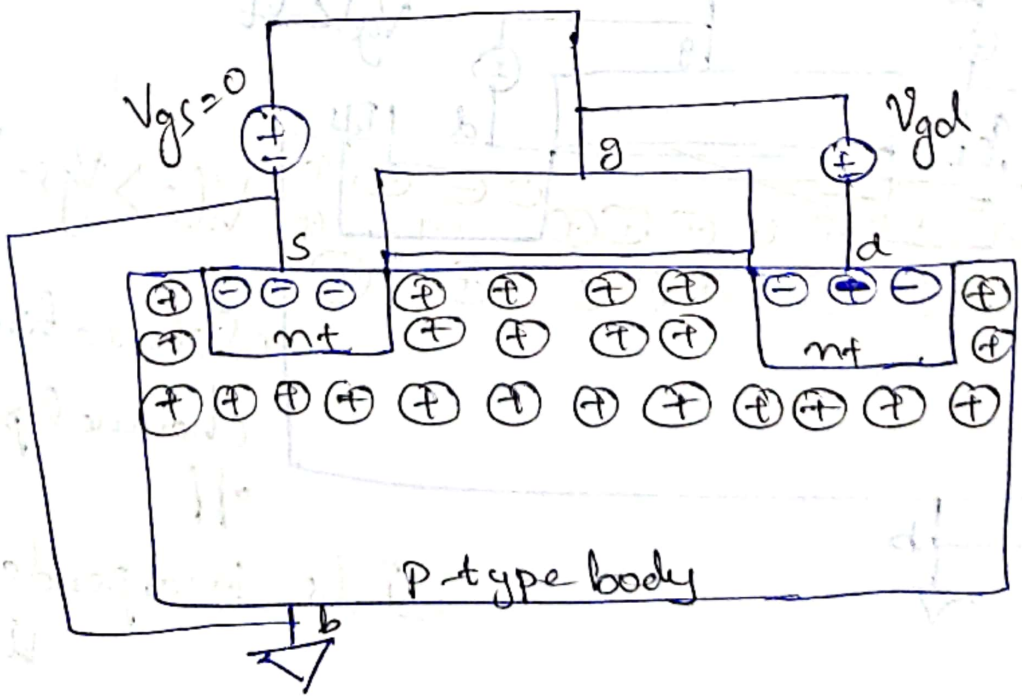
(iii) Under this condition the surface of p-type is inverted to n-type which provides conduction.



2. Derive the expression for Drain to source current for an n-channel MOSFET in all three regions.

(i) Cut-off region.

where the current flow is zero: $I_{ds} = 0V$ and $V_{gs} \leq V_t$

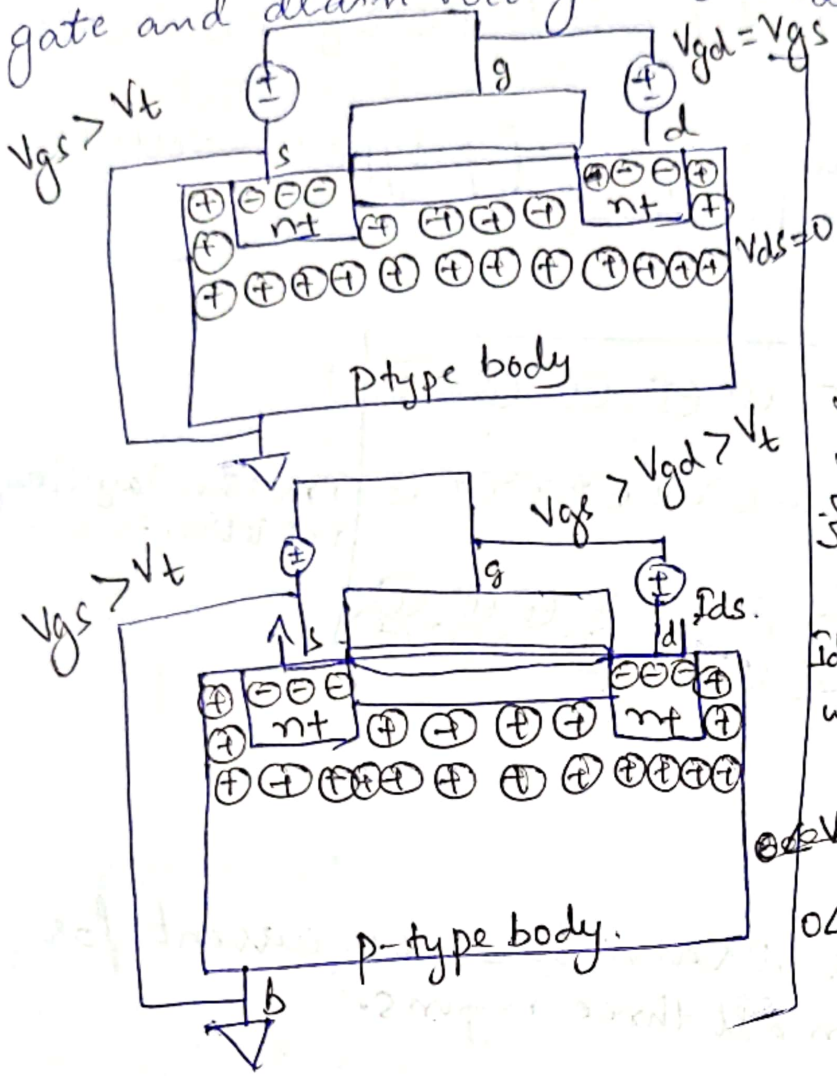


Cutoff: No channel

$I_{ds} = 0$.

(ii) Non-Saturated Region

Weak inversion region where the drain current is depends on gate and drain voltage. $0 < V_{ds} < V_{gs} - V_t$.

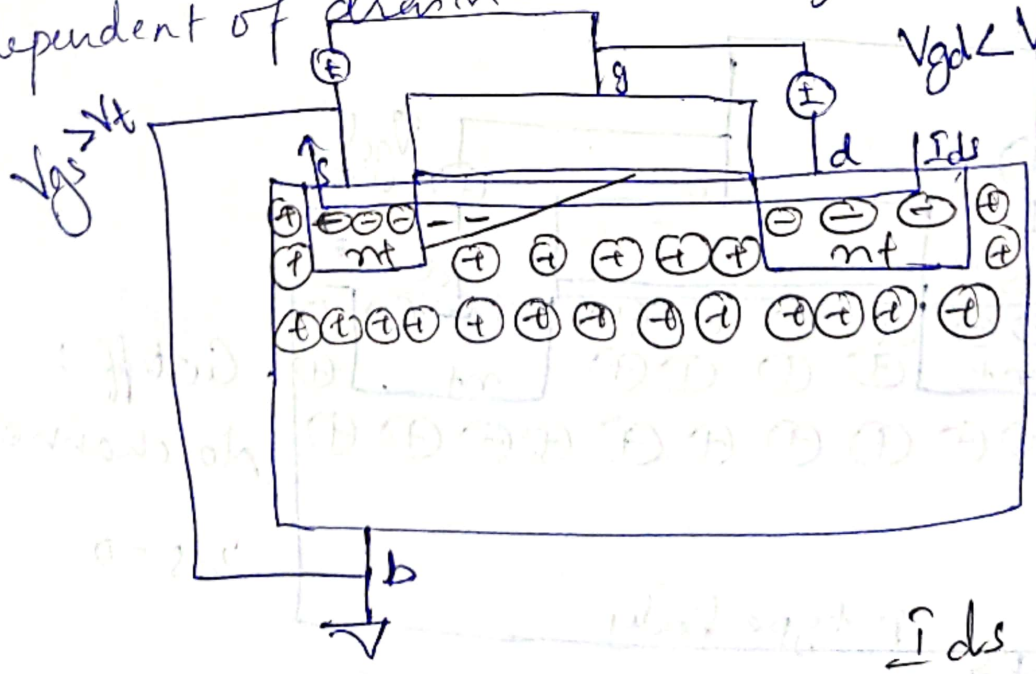


The ideal equation for n-MOS device in three regions are,

$$I_{ds} = \begin{cases} 0; & V_{gs} - V_t \le 0 \quad \text{Cut-off (a)} \\ \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]; & 0 < V_{ds} < V_{gs} - V_t \quad \text{linear (b)} \\ \frac{\beta}{2}(V_{gs} - V_t)^2; & 0 < V_{gs} - V_t < V_{ds} \quad \text{Saturation} \end{cases}$$

(iii) Saturated Regim

Channel in inverted where the drain current is independent of drain source voltage. $0 < V_{gs} - V_t < V_{ds}$



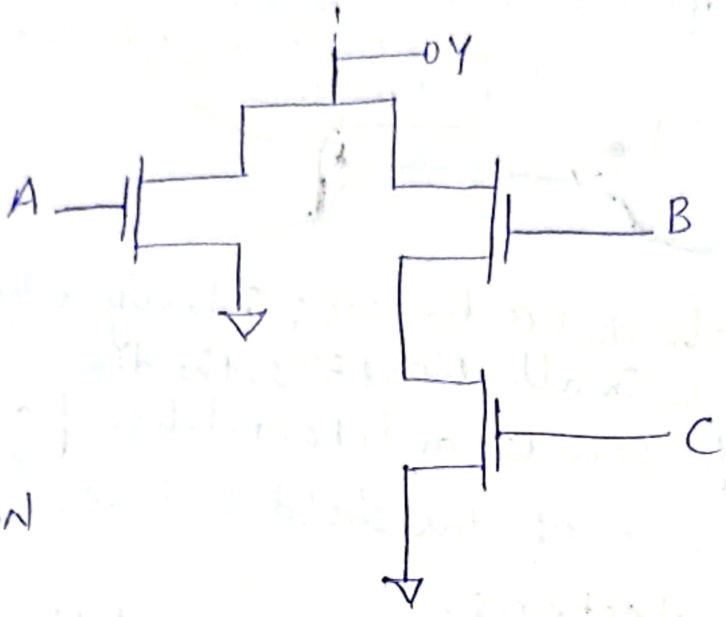
$V_{ds} > V_{gs} - V_t$

Saturation: channel pinches off

I_{ds} independent of V_{ds}.

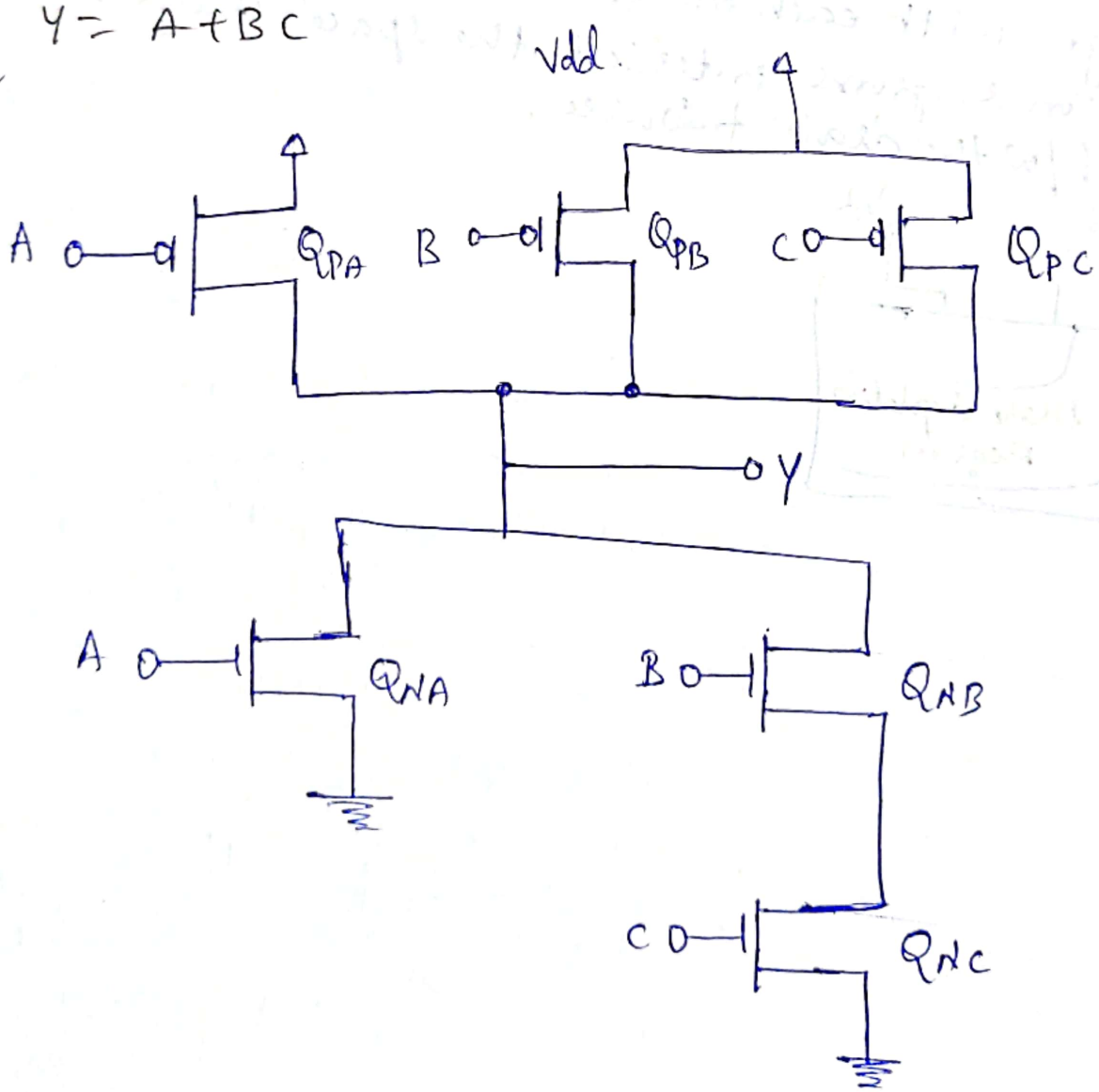
4. Realise the following logic expression using CMOS.

(a) $Y = A + BC$

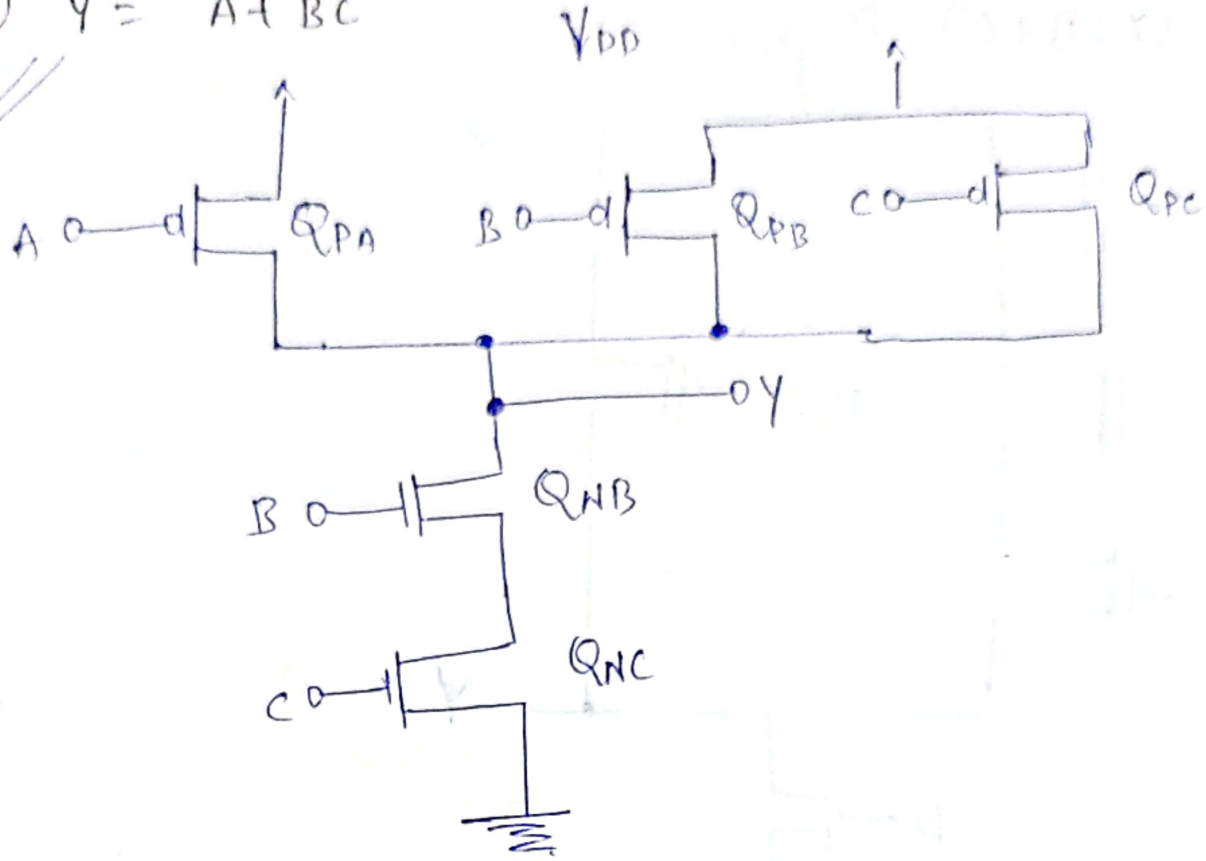


$Y = A + BC$

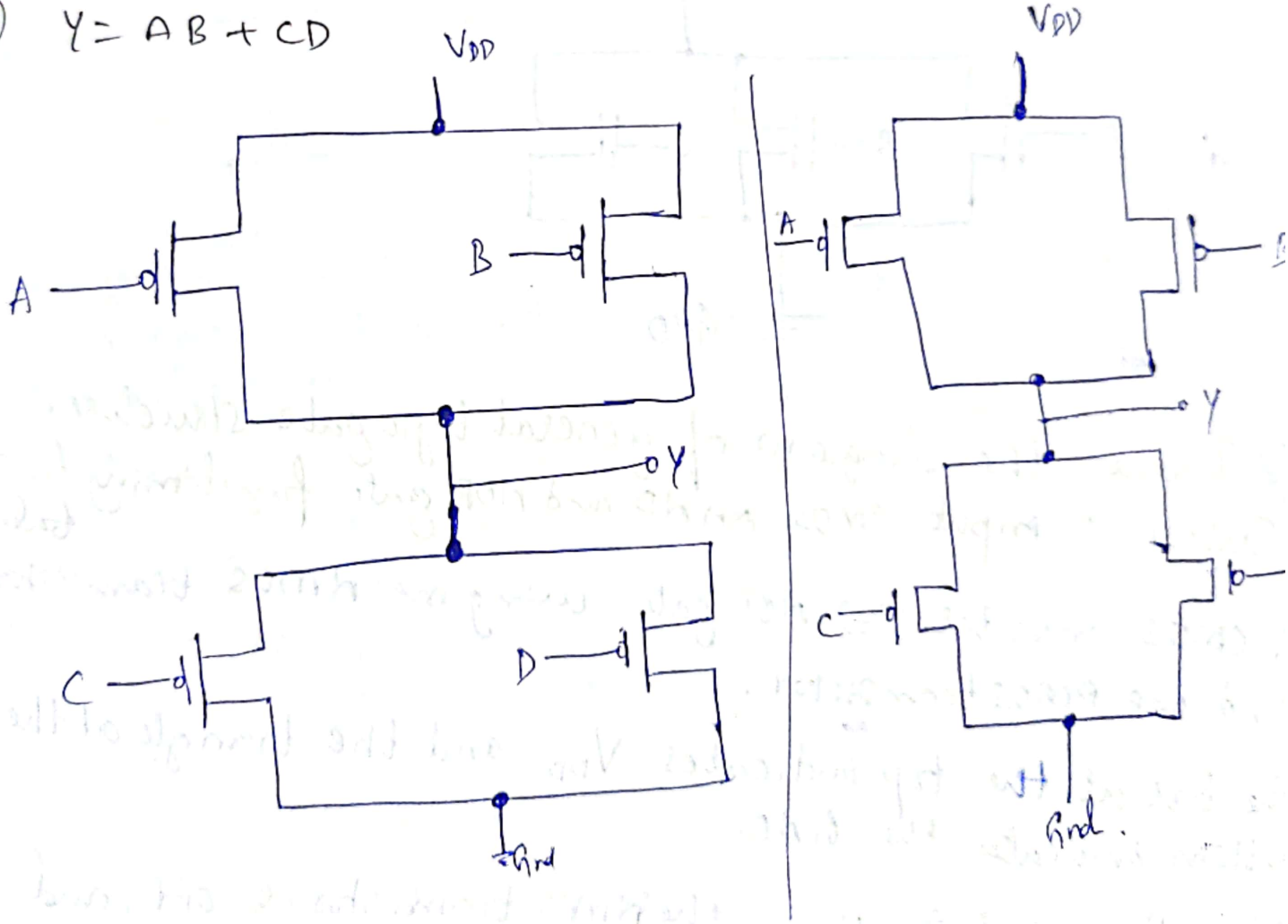
(b) $Y = \overline{A + BC}$



(c) $Y = A + \overline{BC}$



(d) $Y = AB + CD$



* A collection of N flip flop sharing a common clock input is called a Registers.

* A register is often drawn as a flip-flop with multi-bit D and Q buses.

5. Write neat diagrams explain the DC transfer characteristics of CMOS inverter.

Various regions of operation for the n-and p-transistors.

V_{tn} → is the threshold voltage of the n-channel device.

V_{tp} → is the threshold voltage of the p-channel device.

Note that V_{tp} is negative.

The equations are given both in terms of V_{gs} / V_{ds} and V_{in} / V_{out}.

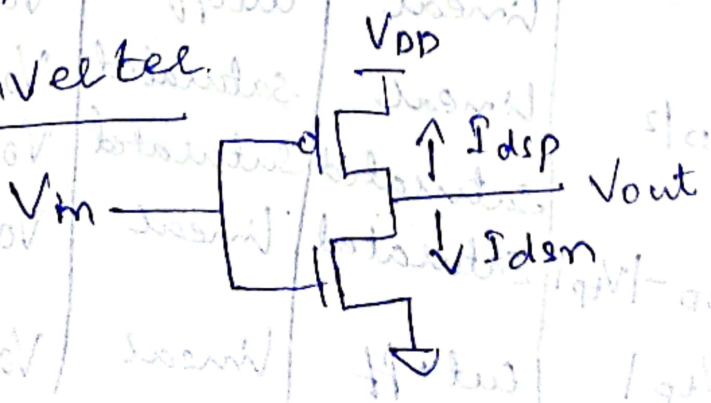
As the source of NMOS transistor is grounded,

$V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$.

As the source of PMOS transistor is tied to V_{DD},

$V_{gsp} = V_{in} - V_{DD}$ and $V_{dsp} = V_{out} - V_{DD}$.

CMOS inverter.



* The operations of the [illegible] divided into five regions.

The state of each transistor in each region.

In region A, the NMOS transistor is OFF so the PMOS transistor pulls the output to V_{DD}.

In region B, the NMOS transistor starts to turn ON, pulling the output down.

In region C, both transistors are in saturation.

Notice that ideal transistors are only in region C for $V_{in} = V_{DD}/2$ and the slope of the transfer curve is $-\infty$ in this region, corresponding to infinite gain.

In region D, the PMOS transistor is partially on.

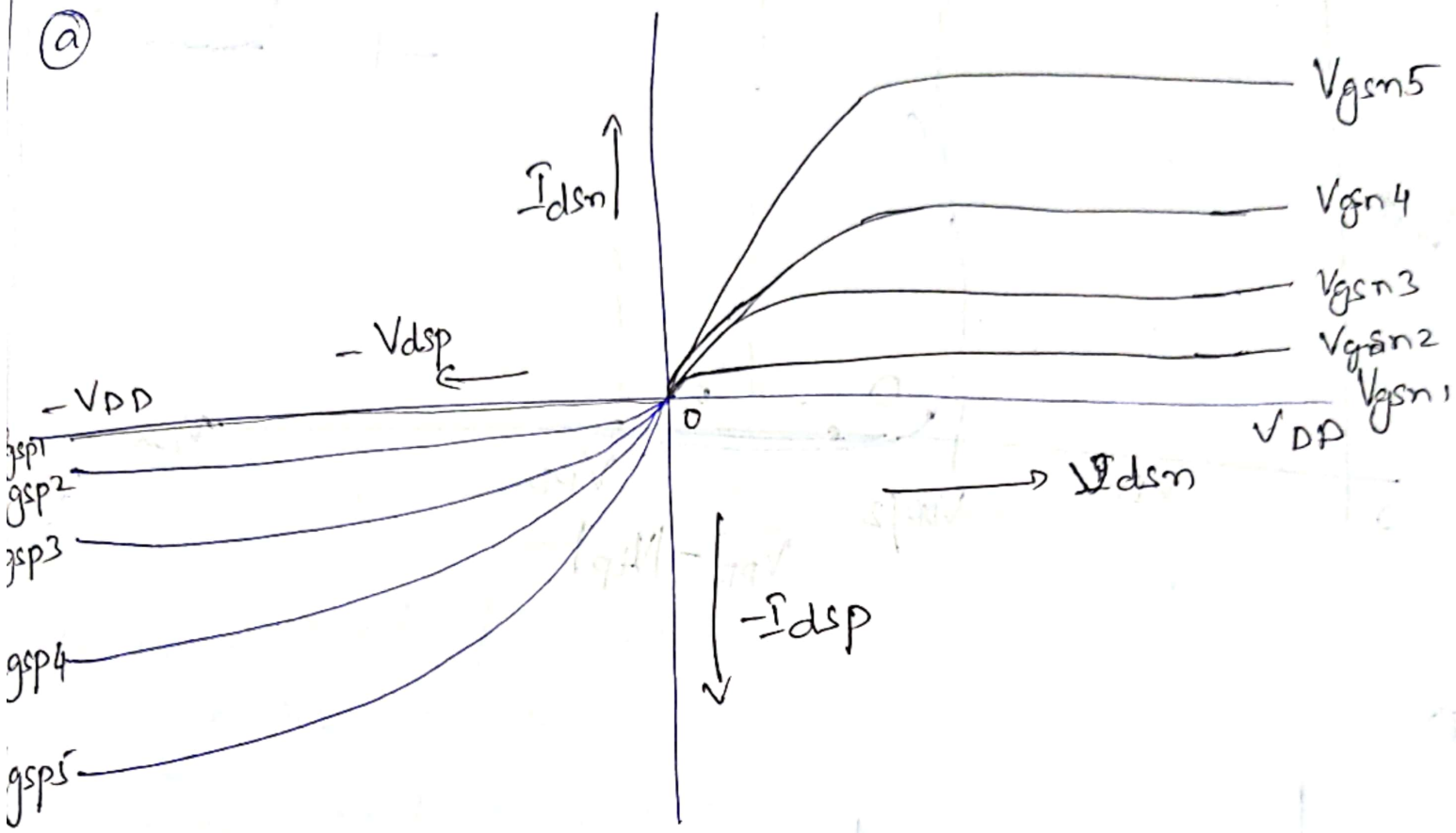
In region E, it is completely off, leaving the NMOS transistor to pull the output down to GND.

Also notice that the inverter's current consumption is ideally zero, neglecting leakage, when the I/P is within the threshold voltage of V_{DD} (or) GND rails
This feature is important for low-power operation.

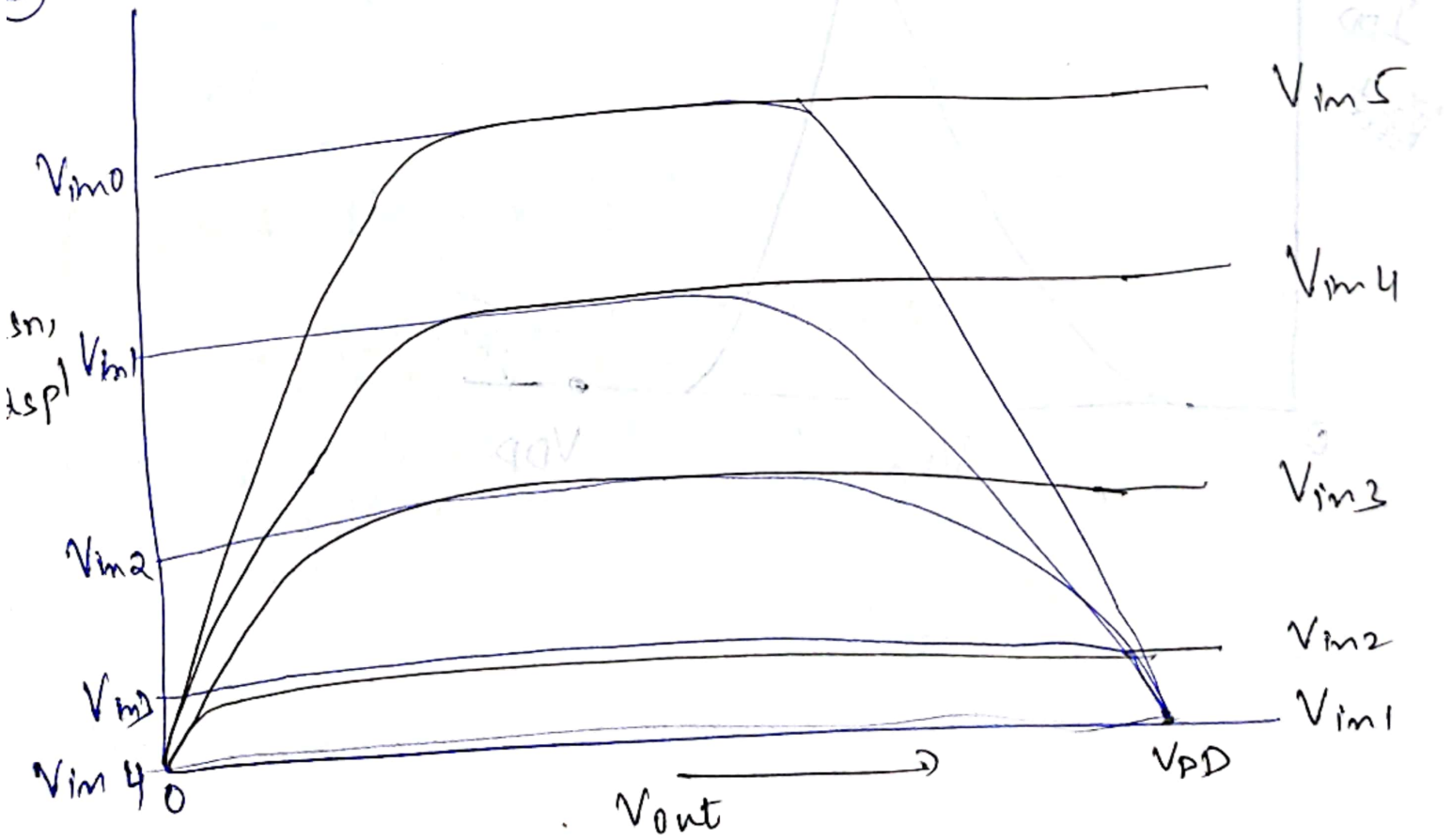
Region	condition	p-device	n-device	O/P
A	$0 \le V_{in} < V_{tn}$	lineal	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	lineal	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	lineal	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cut-off	lineal	$V_{out} = 0$

the cross over point where $V_{inv} = V_{in} = V_{out}$ is called i/p threshold.

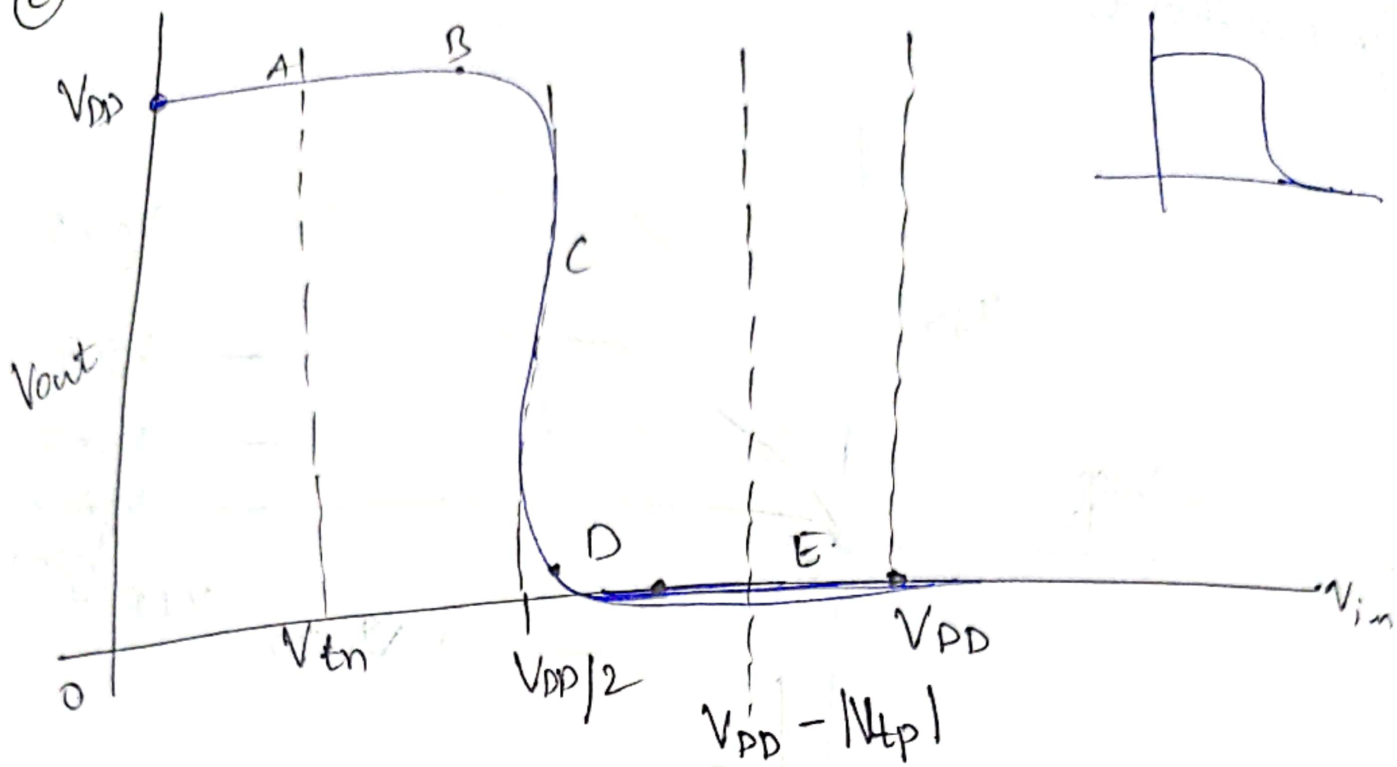
(a)



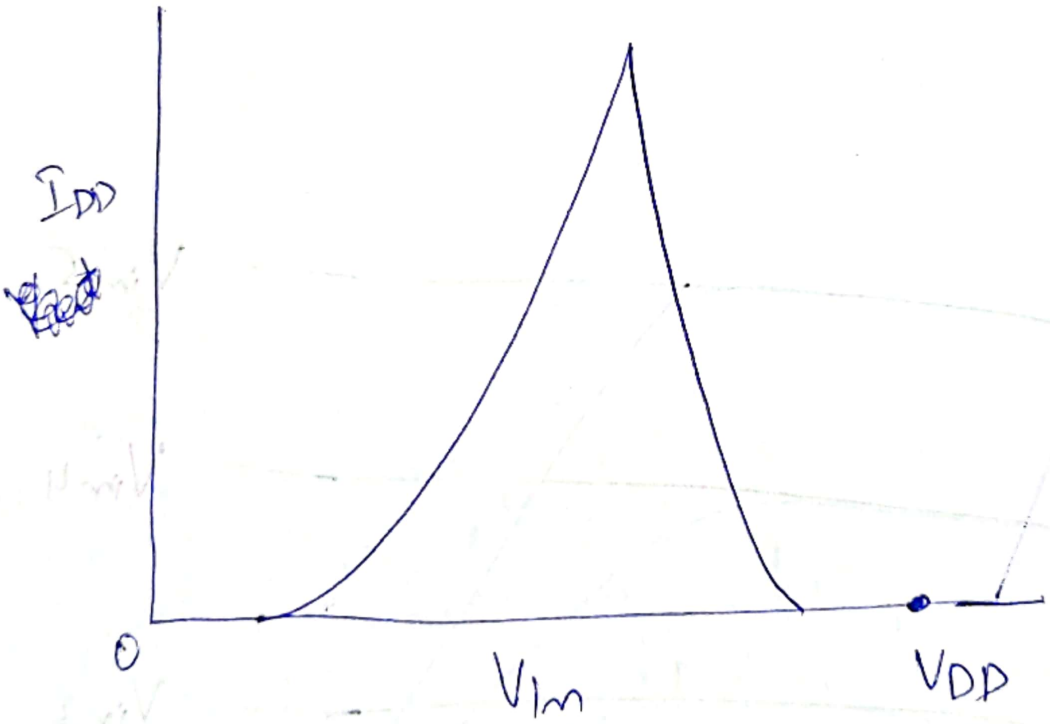
(b)



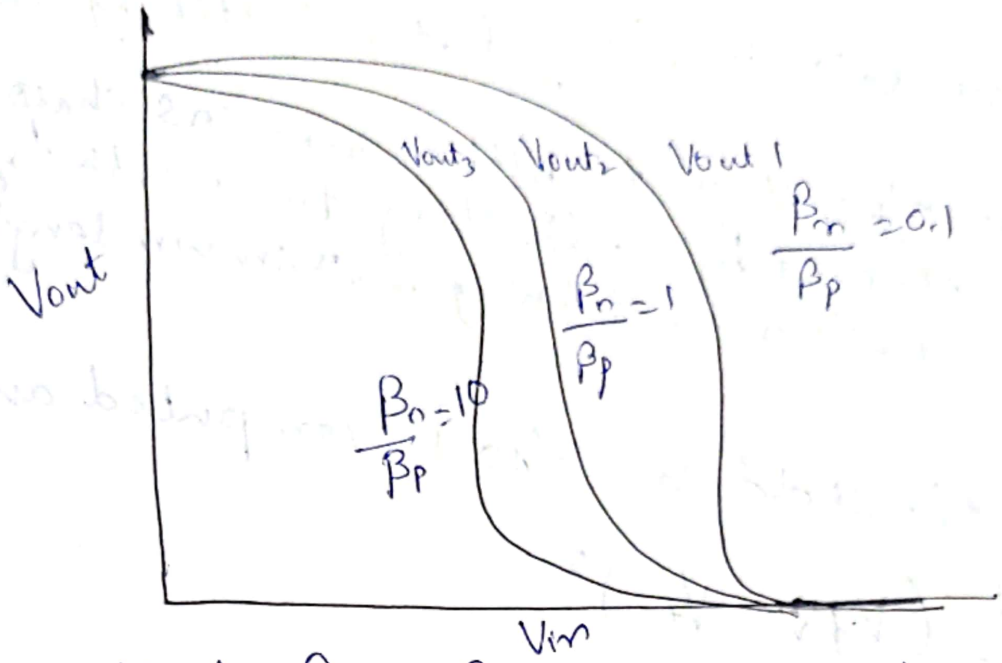
(c)



(d)



9. Explain the effects of β_n / β_p ratio variations in the transfer characteristics of CMOS inverter with neat diagram.



We know that $\beta_p = \beta_n$, the inverter threshold voltage V_{inv} is $V_{DD}/2$.

Inverter with different beta ratios $r = \frac{\beta_p}{\beta_n}$ are called skewed inverter [Sutherland

If $r > 1$, the inverter is HI-skewed.

If $r < 1$, the inverter is LO-skewed.

If $r = 1$, the inverter has normal skew (or) is unskewed.

A HI-skew inverter has a stronger PMOS transistor. Therefore, if the i/p is $V_{DD}/2$, the o/p will be greater than $V_{DD}/2$.

In other words, the i/p threshold must be higher th

Similarly, a LO-skew inverter has a weaker PMOS transistor and thus a lower switching threshold.

As the beta ratio is changed, the switching threshold moves.

However, the o/p voltage transition remains sharp. Gates are usually skewed by adjusting the widths of transistors while maintaining minimum length for speed.

The inverter threshold can also be computed analytically

$$I_{dn} = \frac{\beta_n}{2} (V_{inv} - V_{tn})^2$$

$$I_{dp} = \frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2.$$

By setting the currents to be equal & opposite.

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

transistors are fully velocity saturated.

$$I_{dn} = W_n C_{ox} v_{sat-n} (V_{inv} - V_{tn})$$

$$I_{dp} = W_p C_{ox} v_{sat-p} (V_{inv} - V_{DD} - V_{tp}).$$

Redefining $r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}}$,