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CMR INSTITUTE OF TECHNOLOGY

Internal Assesment Test – II									
Sub:	**VLSI DESIGN & TESTING**							**Code:**	**21EC63**
Date:	**09.07.2024**	**Duration:**	**90 mins**	**Max Marks:**	**50**	**Sem**	**VI**	**Branch**	**ECE-A,B,C,D**

Answer Any Five Questions

	Questions	Marks	OBE	
			CO	RBT
1.	With neat diagrams explain n-well CMOS fabrication process.	[10]	CO2	L1
2.	Draw the stick and layout diagram for the function $Y = \overline{ABC + D}$.	[10]	CO2	L2
3.	Construct necessary equivalent circuits using RC delay model to compute the propagation delay of 3-input NAND Gate.	[10]	CO2	L2

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4.	Make use of necessary circuit diagrams to compute logical effort of the following gates. (i) 2-input NOR gate and (ii) 3-input NAND Gate.	[10]	CO2	L2
5.	With necessary circuit diagram, explain the operation of three transistor DRAM cell.	[10]	CO3	L2
6.	Explain full CMOS SRAM cell with necessary circuit topology.	[10]	CO3	L2

CI **CCI** **HOD**

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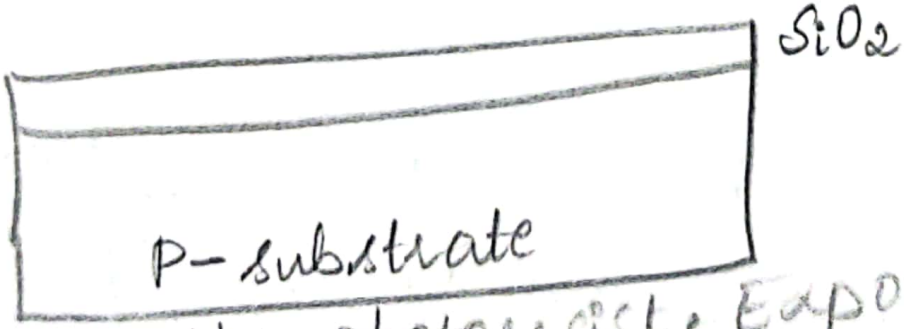
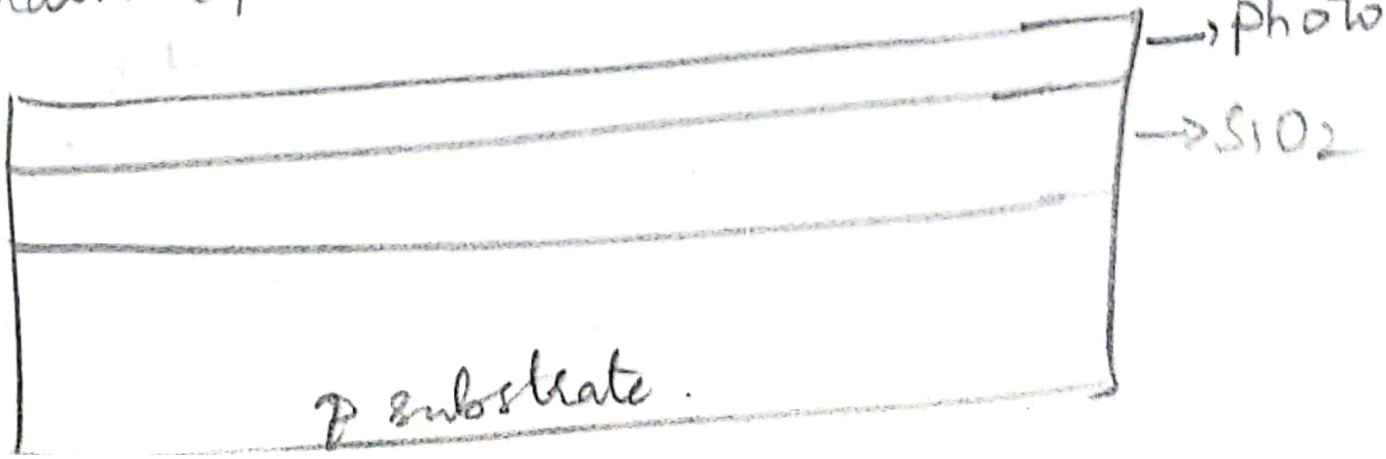
CI **CCI** **HOD**

7. Explain neat diagram explain n-well cmos fabrication process.

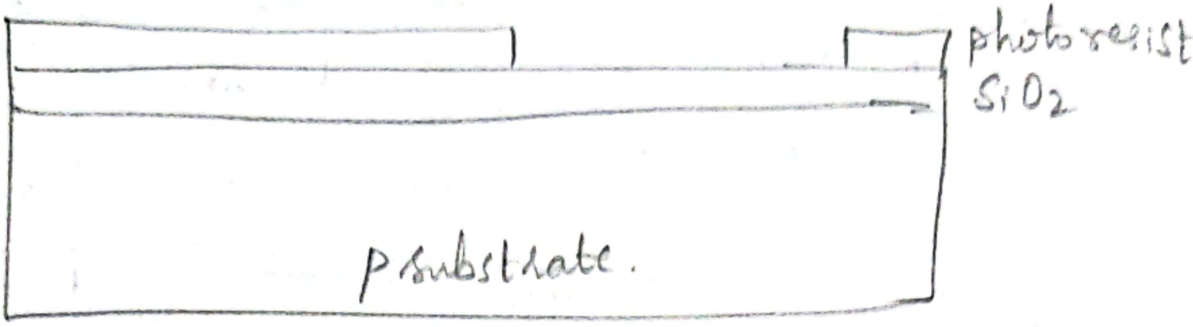
(a) Blank wafer covered with a layer of SiO_2 using oxidation.



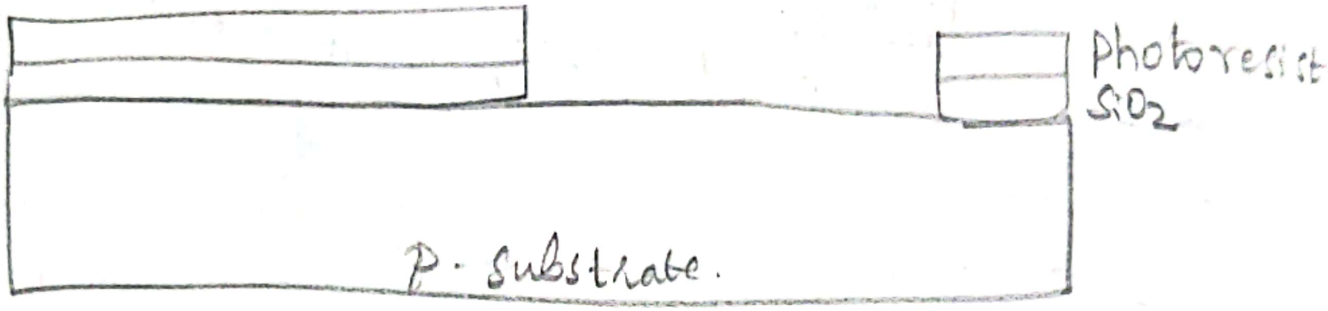
(b) Spin on the photoresist. Exposed to UV light using the n-well mask. (photo lithography)



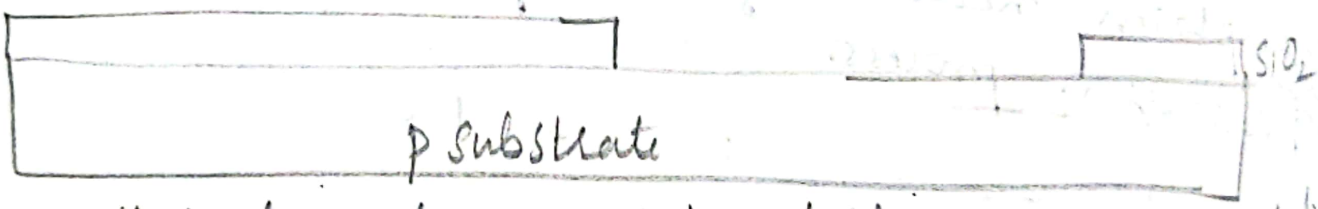
(c) Strip off the exposed photoresist using organic solvents.



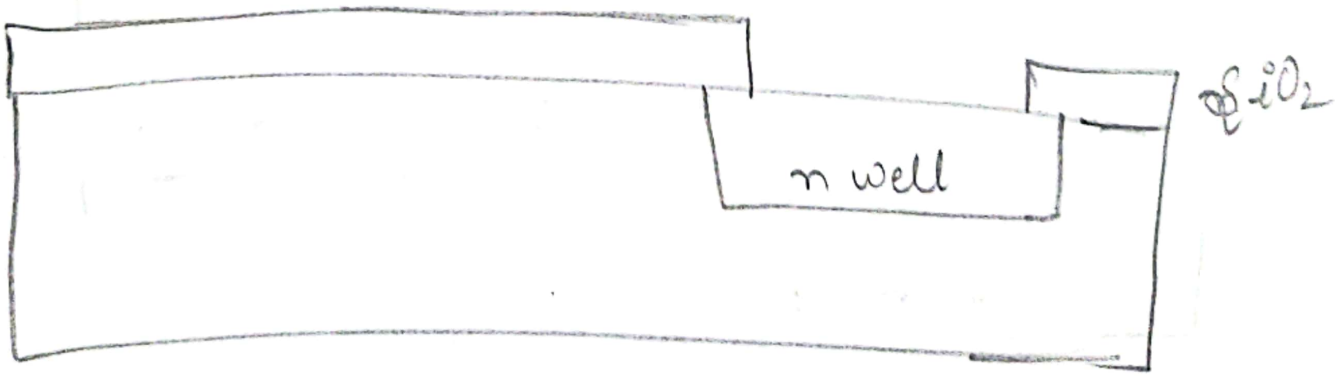
(d) Etch the uncovered oxide using HF (Hydro flowric acid)



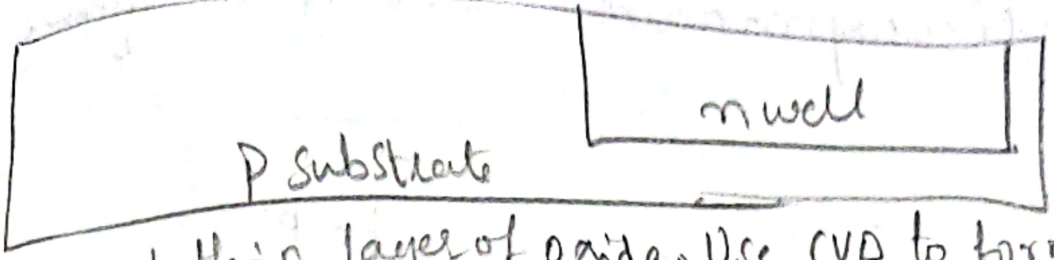
(e) Etch the remaining photoresist using a mixture of ac



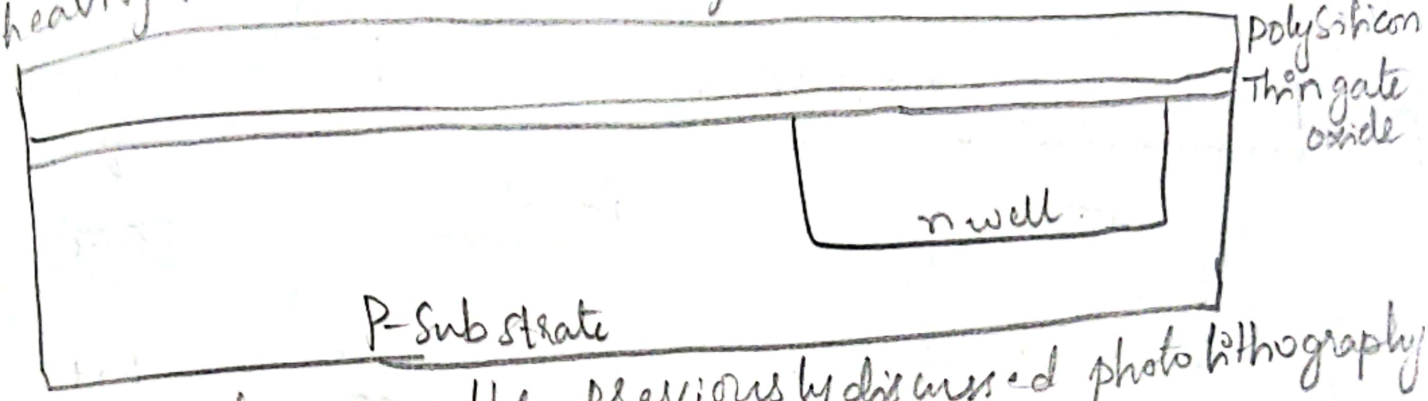
(f) n-well is formed using either diffusion or ion implantation



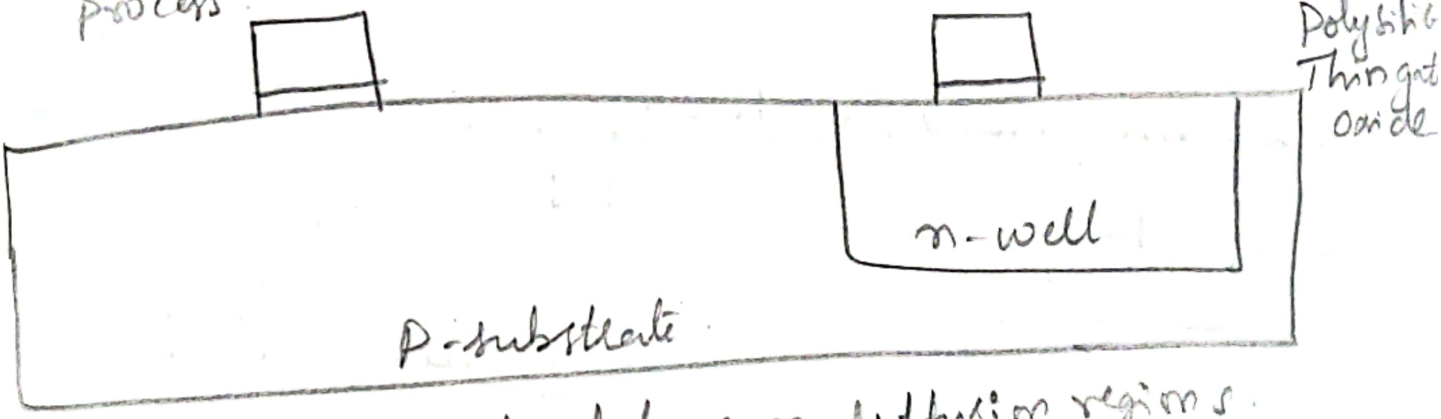
(g) Strip off the remaining oxide using HF. Subsequent steps use the same photolithography process.



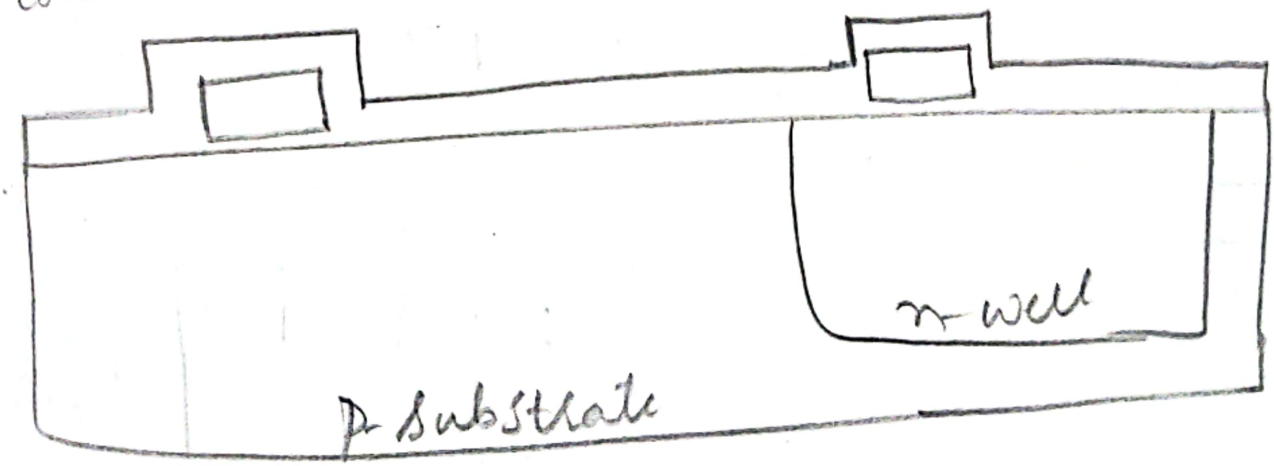
4) Deposit thin layer of oxide. Use CVD to form poly and dope heavily to increase conductivity



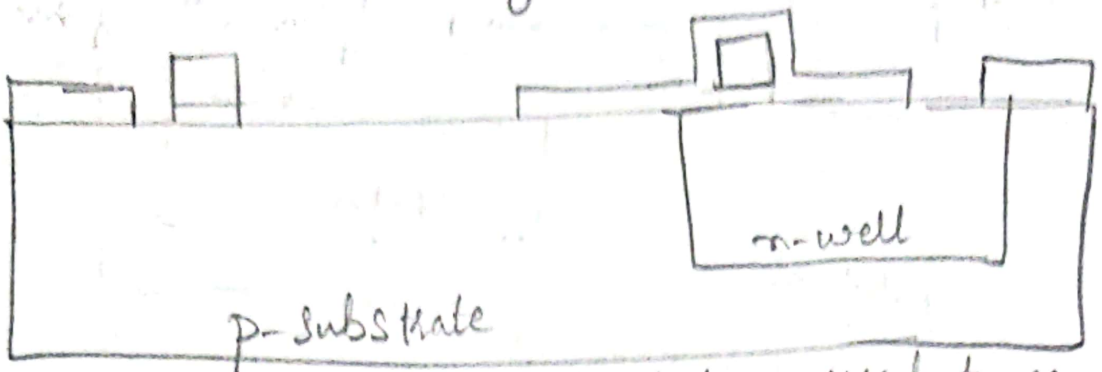
5) Pattern poly using the previously discussed photolithography process



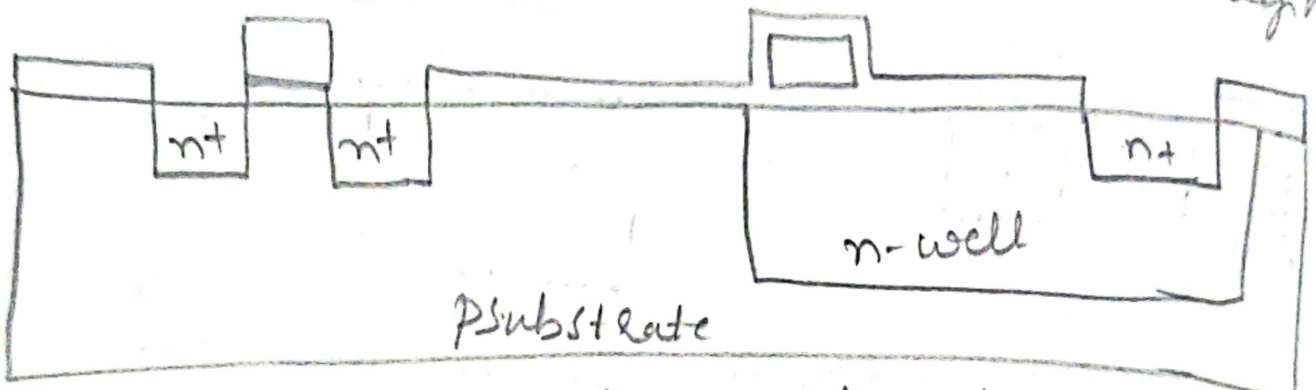
6) Cover with oxide to define n diffusion regions.



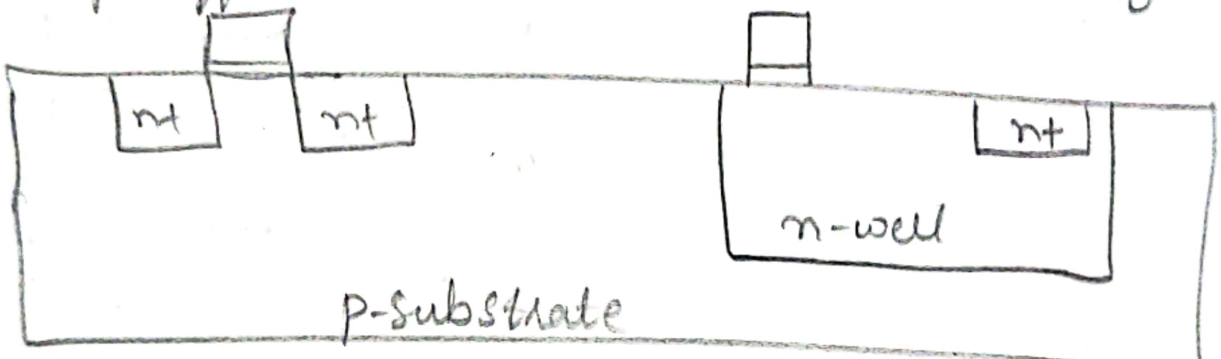
(k) Pattern oxide using n+ active mask to define n diffusion regions



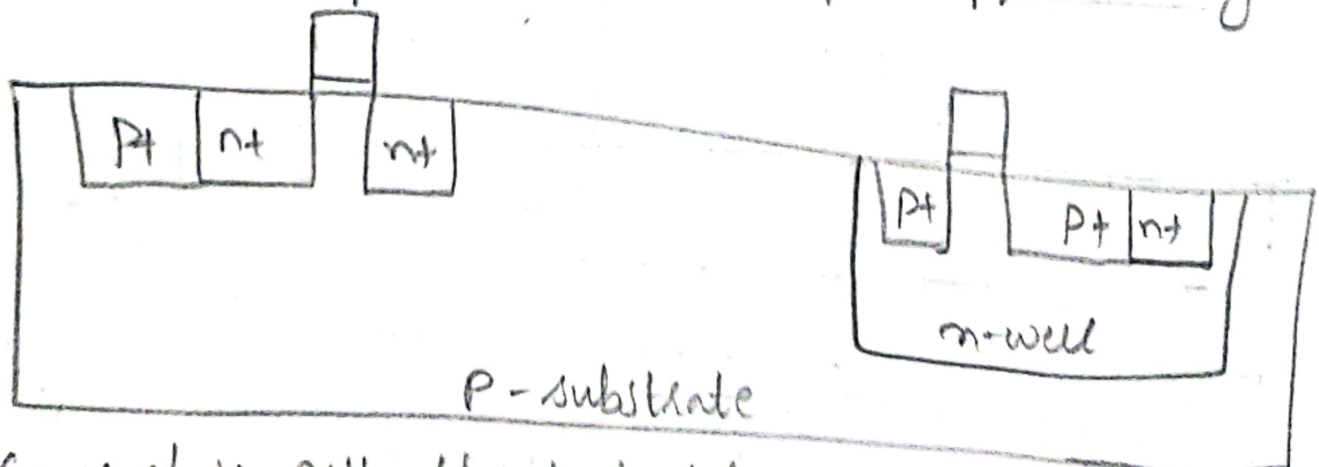
(l) Diffusion (or) ion implantation used to create n diffusion region



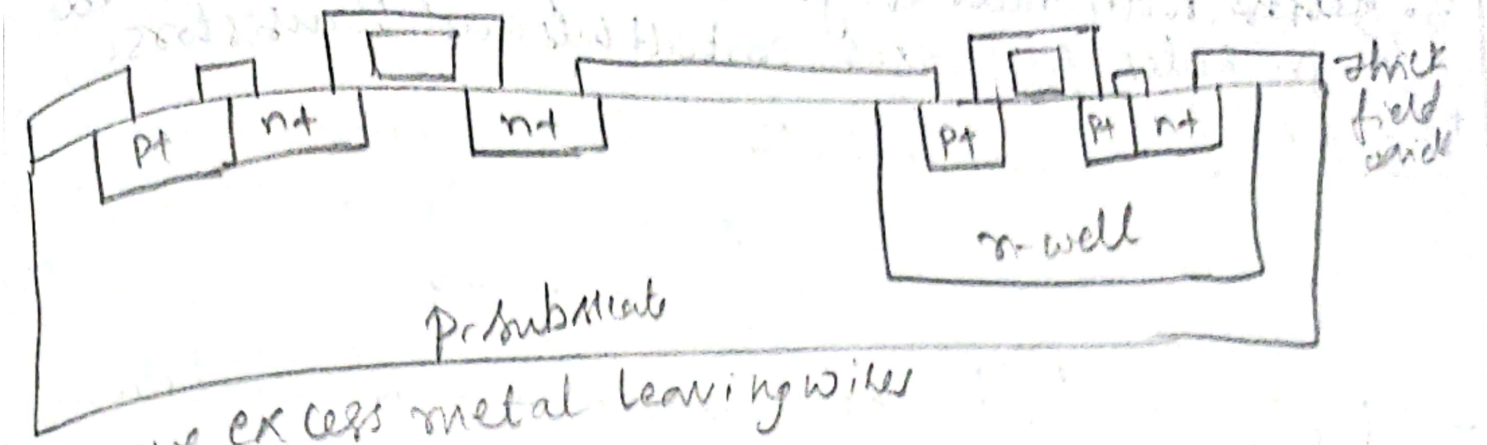
(m) Strip off the oxide to complete patterning step



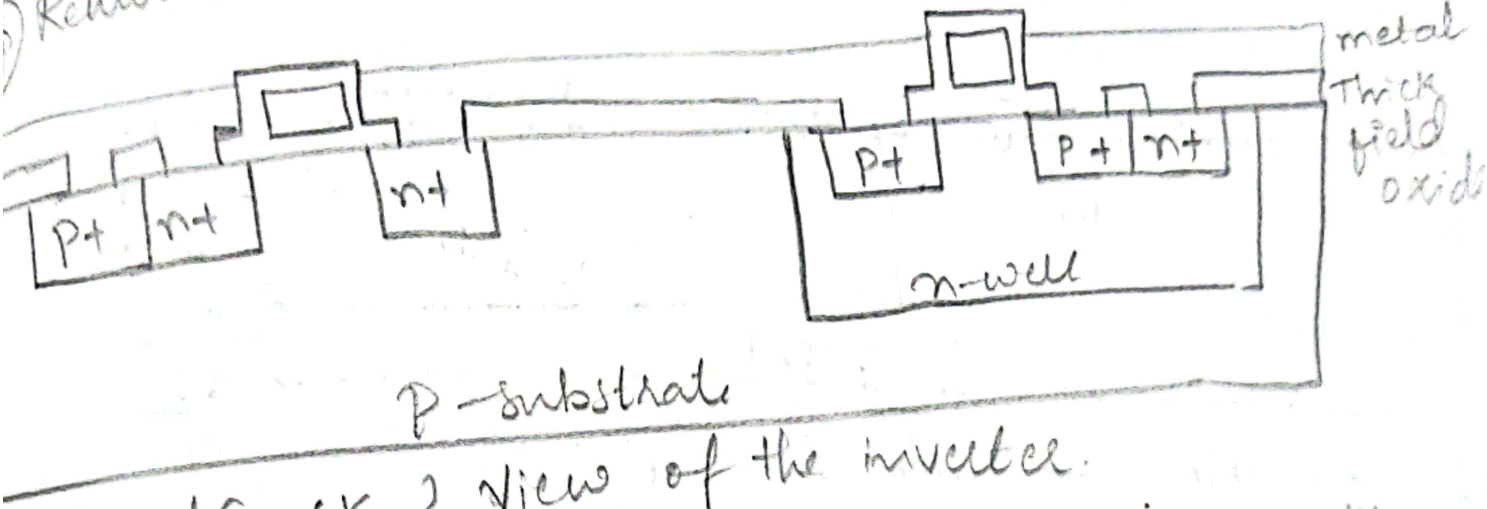
(n) Similar steps used to create p-diffusion regions



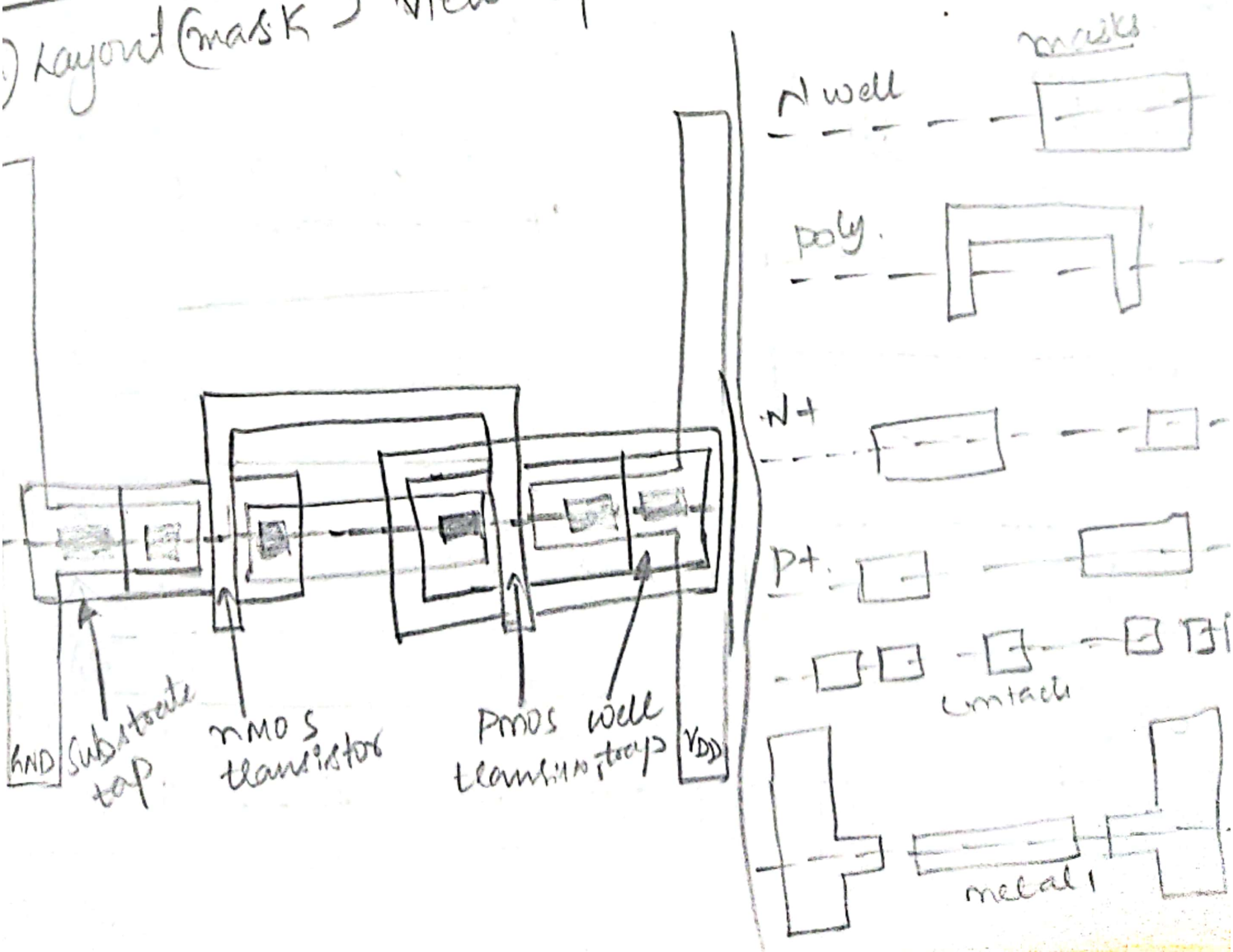
(o) Cover chip with thick field oxide and etch oxide where contact cuts are needed.



c) Remove excess metal leaving wires



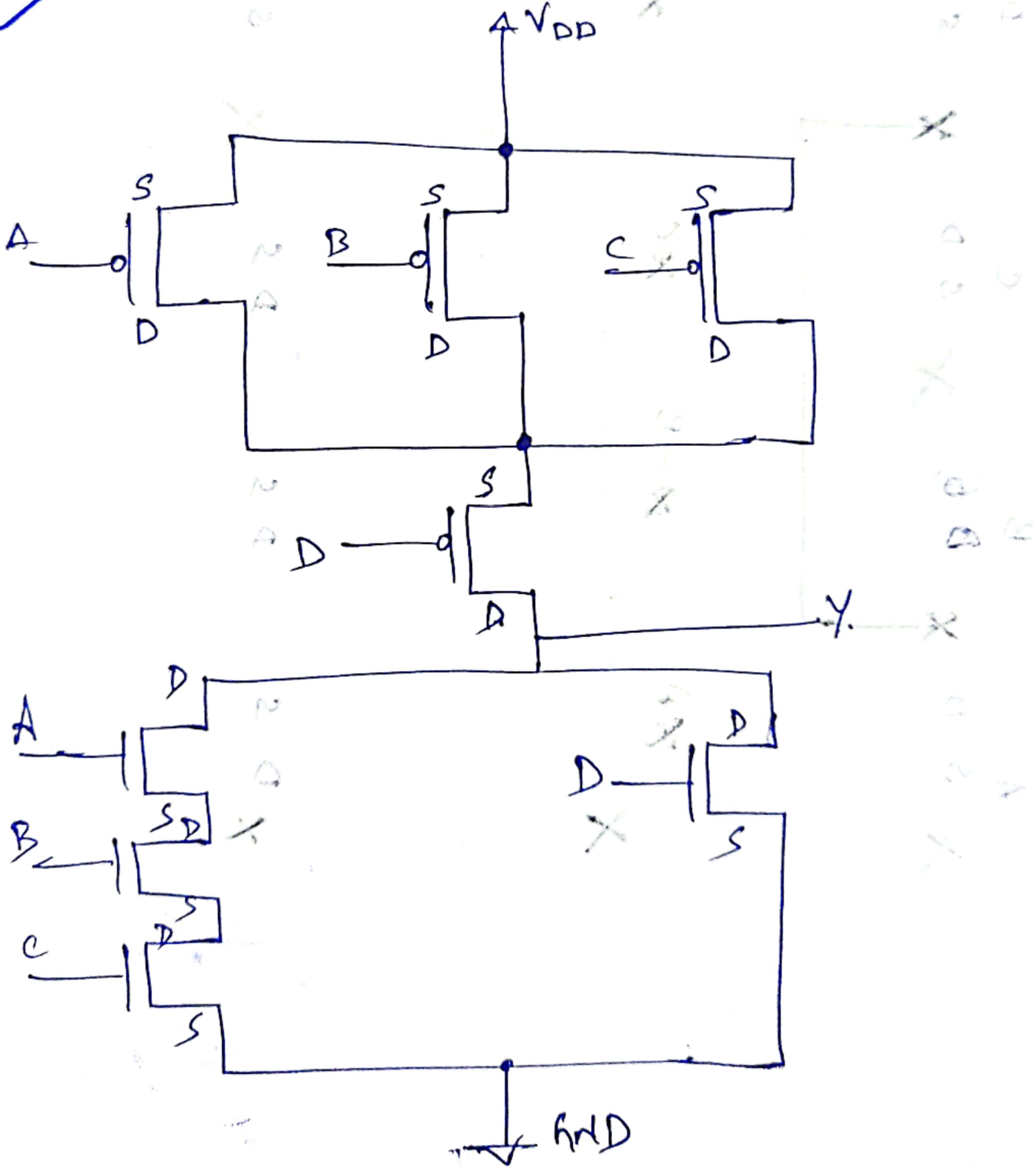
d) Layout (mask) view of the inverter.

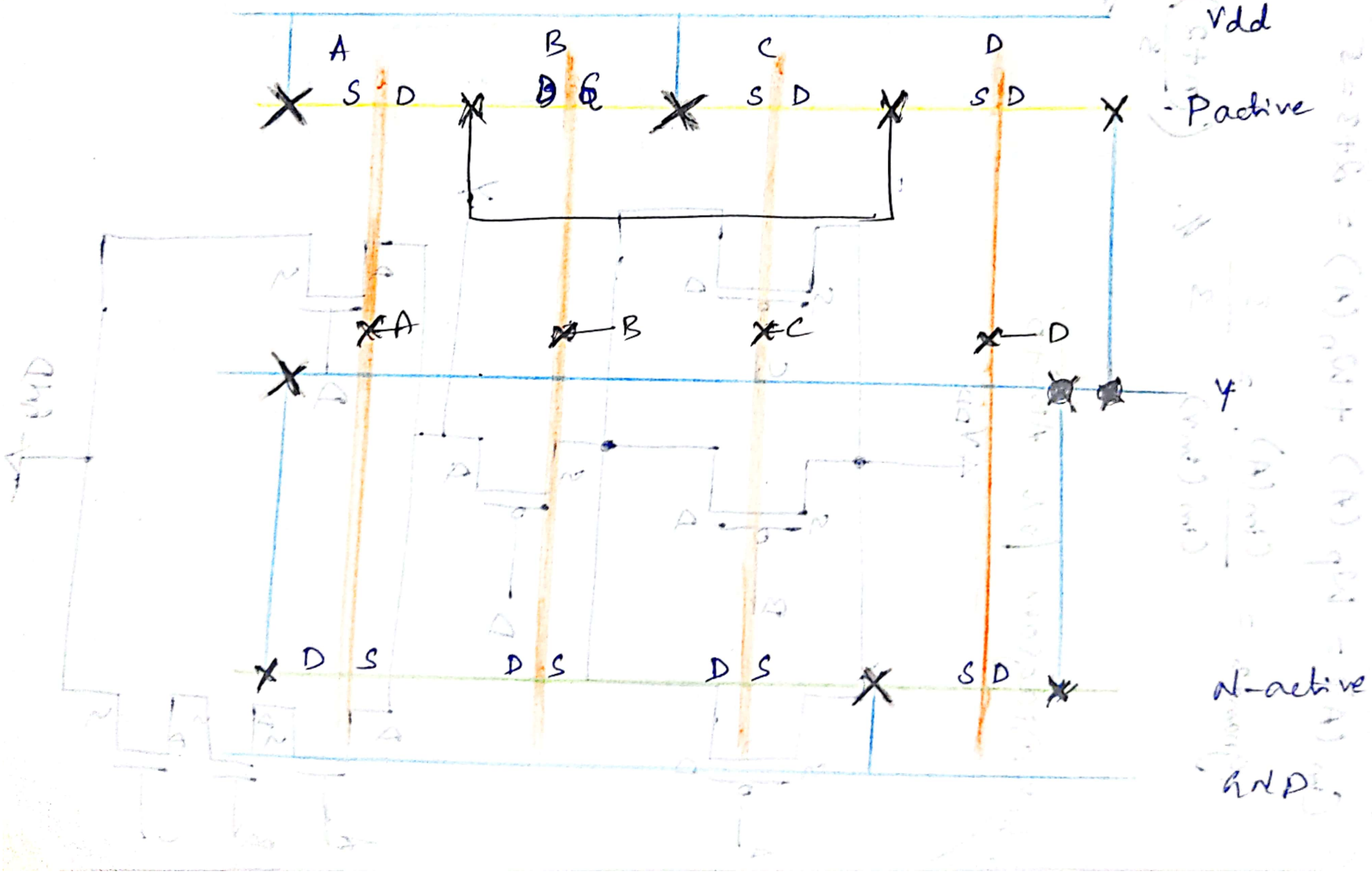


$C_{in}(A) = W_p(A) + W_n(A) = 2+3 = 5$

$g_{nand3} = \frac{C_{in}(A)}{C_{in}(inv)} = \frac{5}{3}$ 4. $\left(\frac{(n+2)}{3}\right)$

4. Stick Diagram for $\overline{ABC+D}$





2. Construct necessary equivalent circuits using RC delay model to compute the propagation delay of 3-input NAND gate.

RC circuit models for nMOS and pMOS transistors with width k with contacted diffusion on both source and drain.

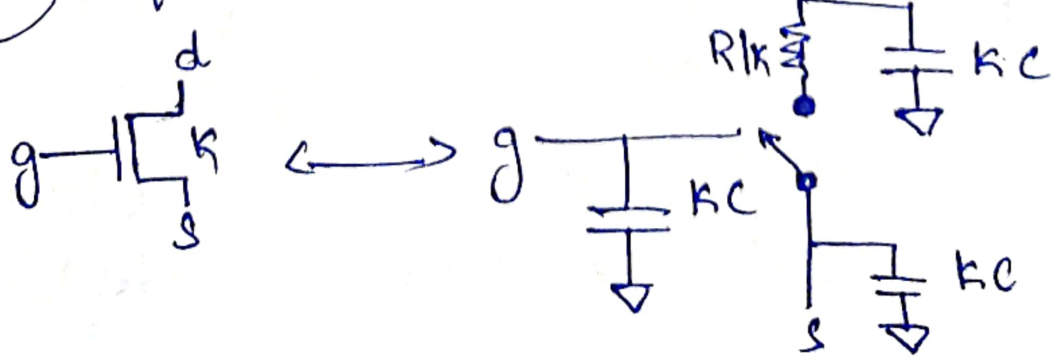
The PMOS transistor has approximately twice the resistance of the NMOS transistor because holes have lower mobility than electrons.

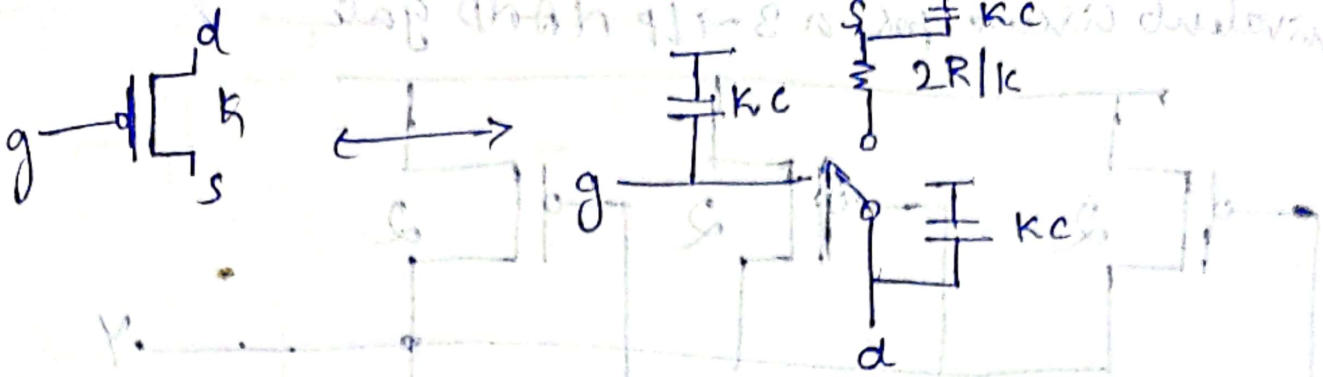
The PMOS capacitors are shown with V_{DD} as their terminal because the n-well is usually tied high

The equivalent circuits for logic gates are assembled from the individual transistors.

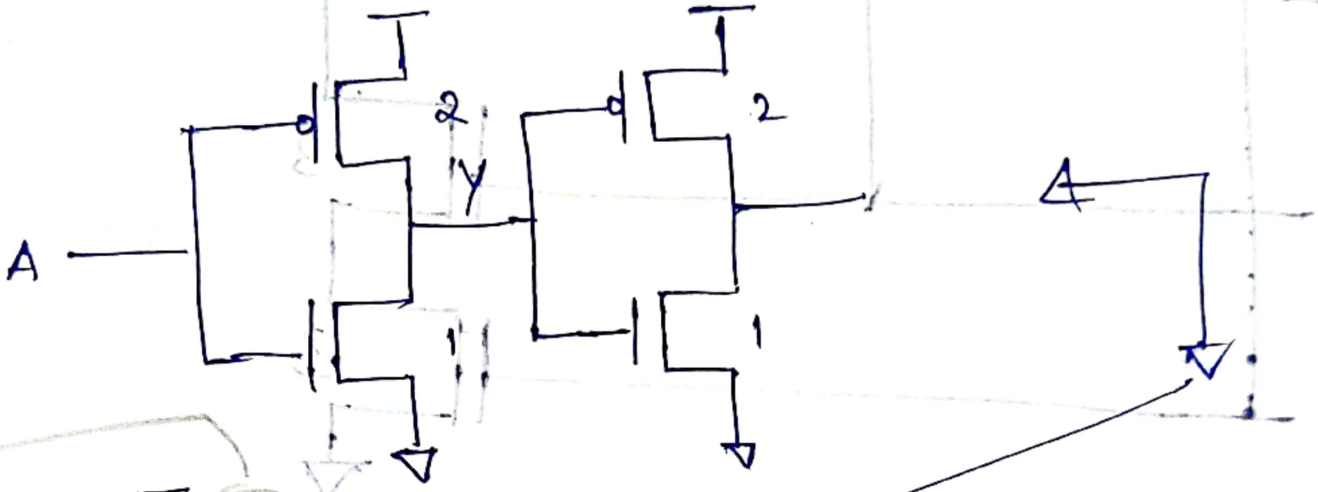
The unit inverters are composed from an NMOS transistor of unit size and a PMOS transistor of twice unit width to achieve equal rise and fall resistance

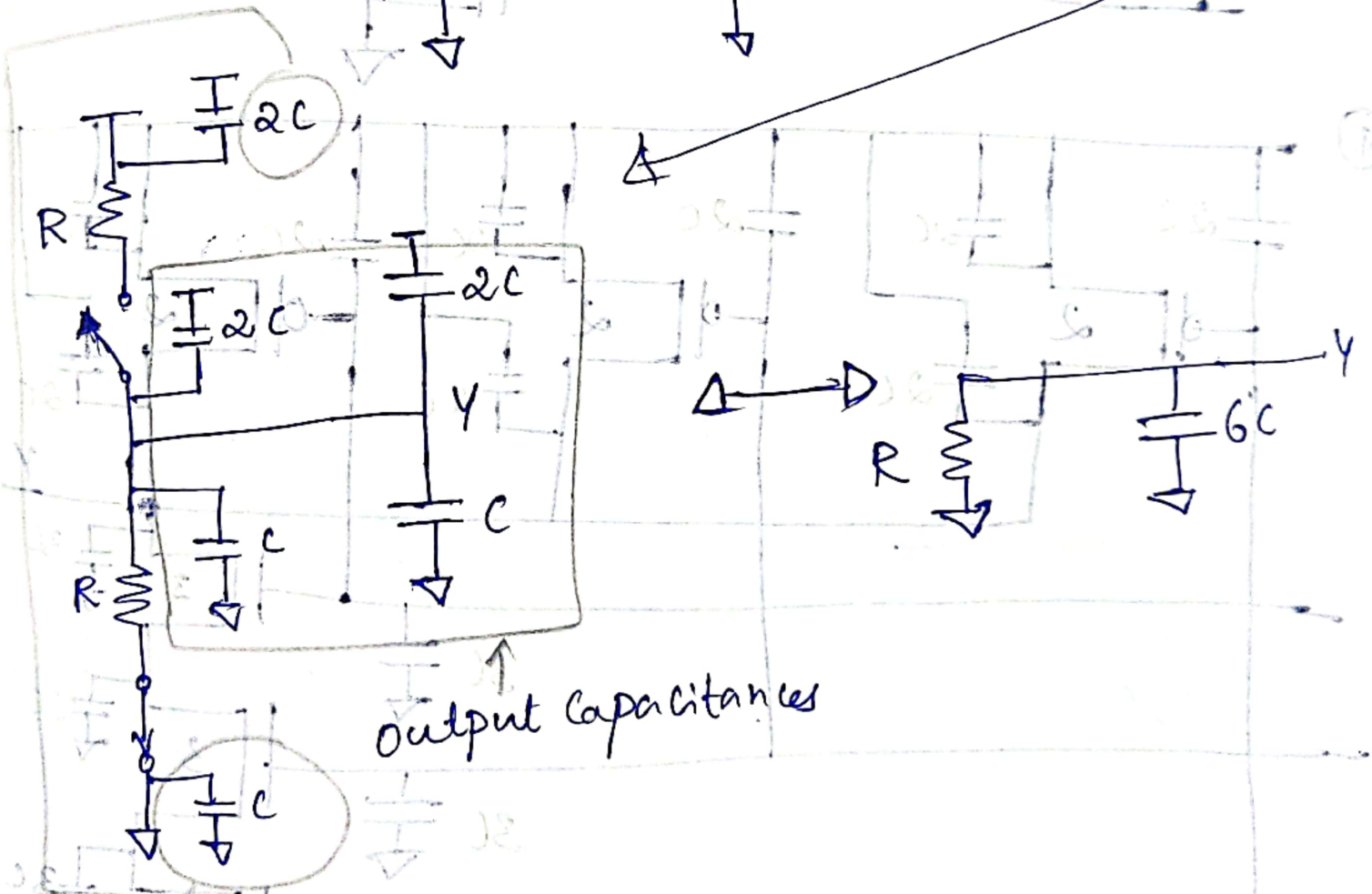
(a) Equivalent circuits for d transistors.





(b) Equivalent circuit for an inverter.



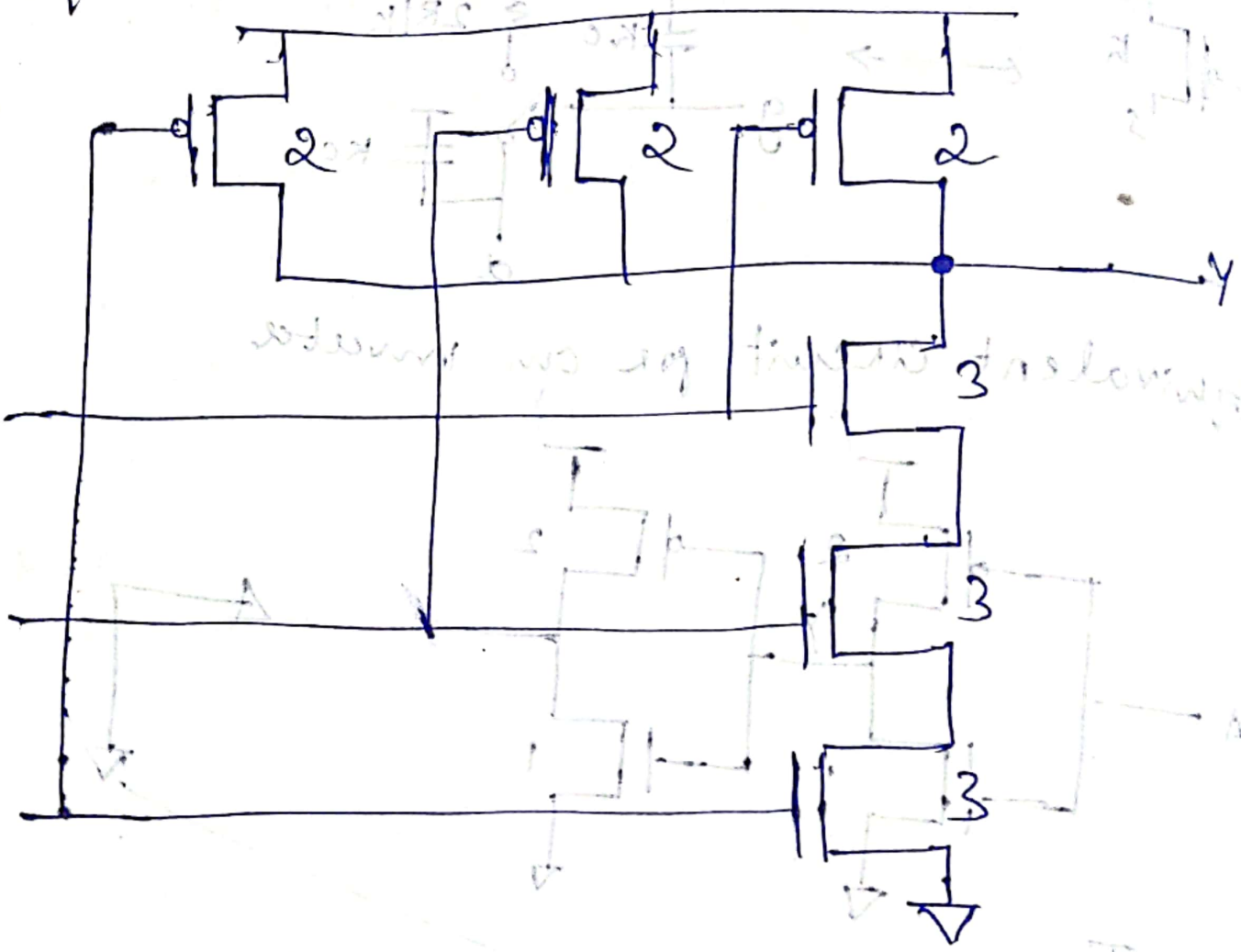


output capacitances

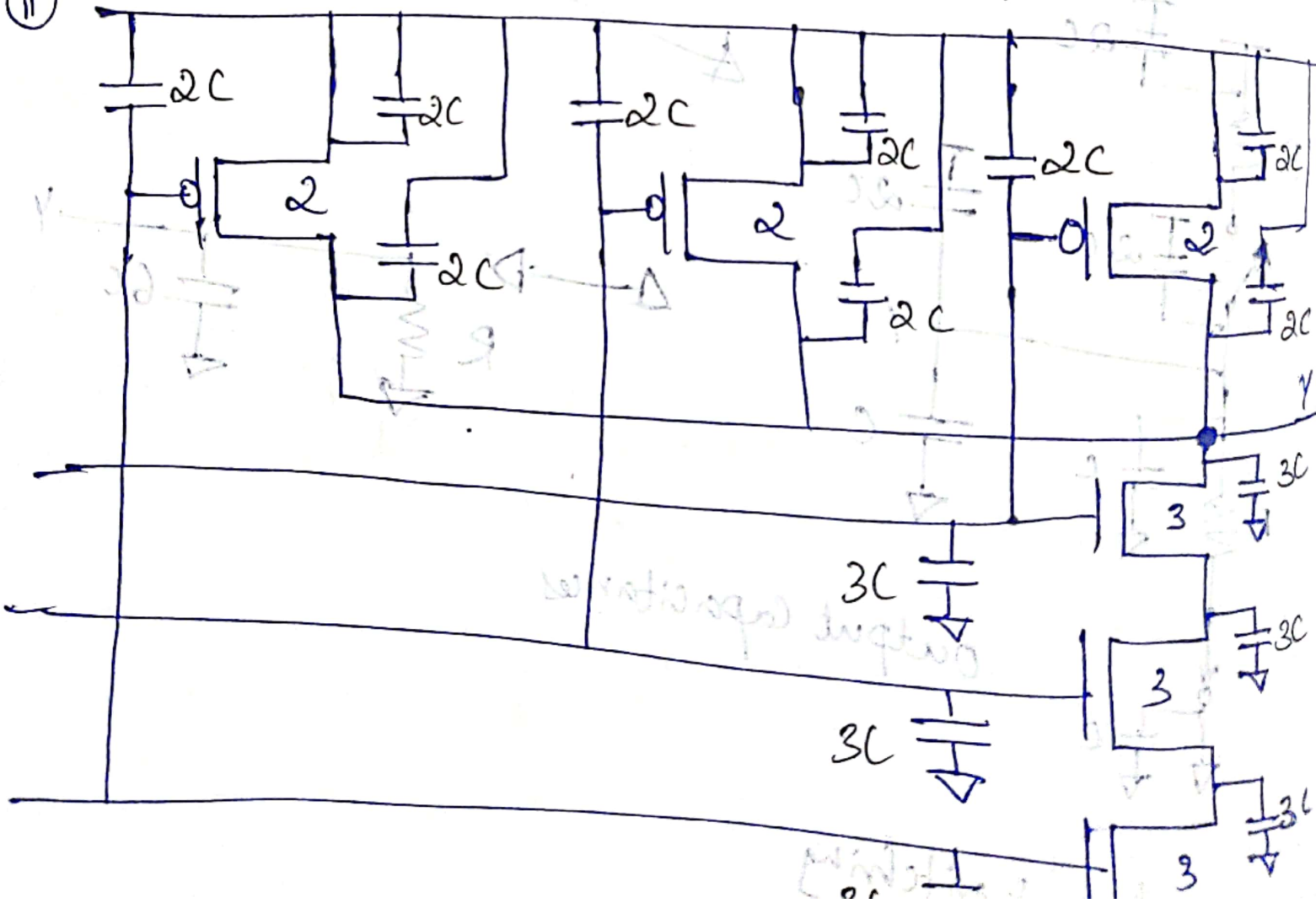
Non-switching capacitance is irrelevant

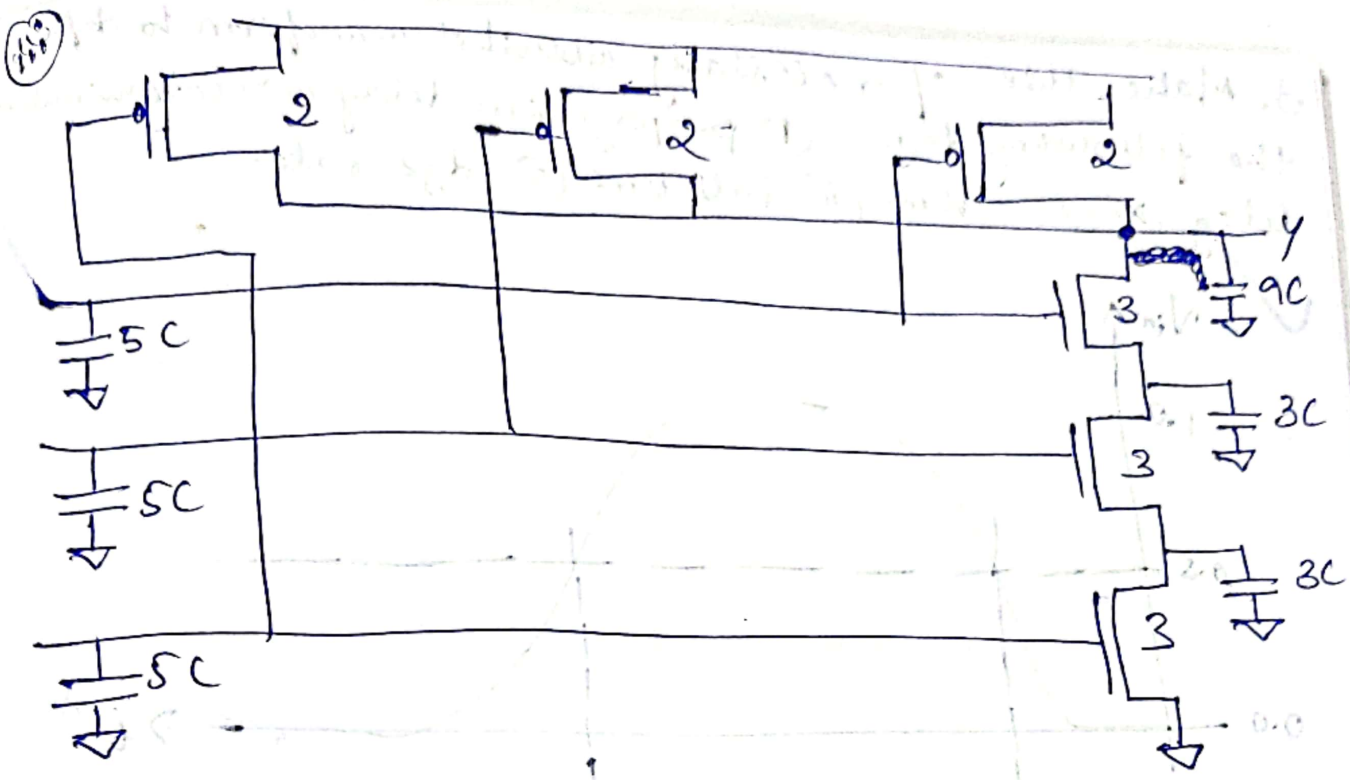
(c) Equivalent circuit for a 3-i/p NAND gate

(i)

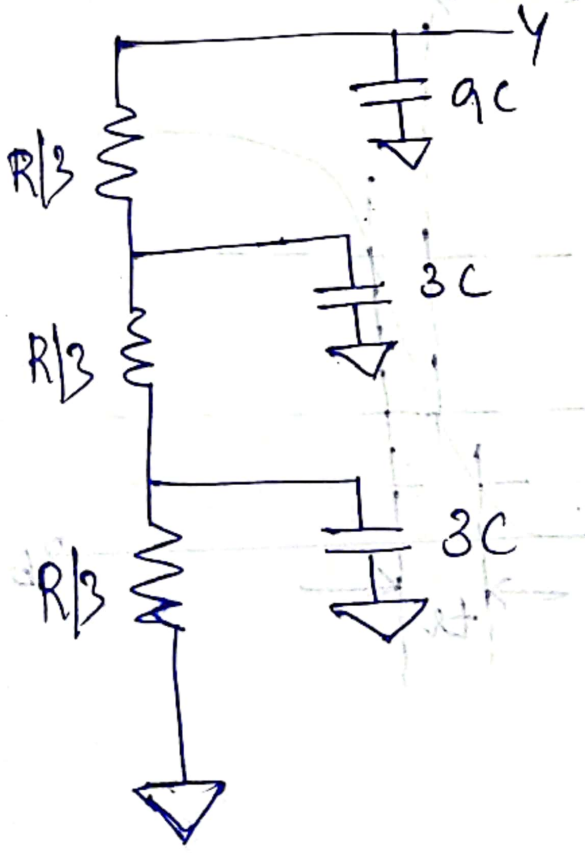


(ii)

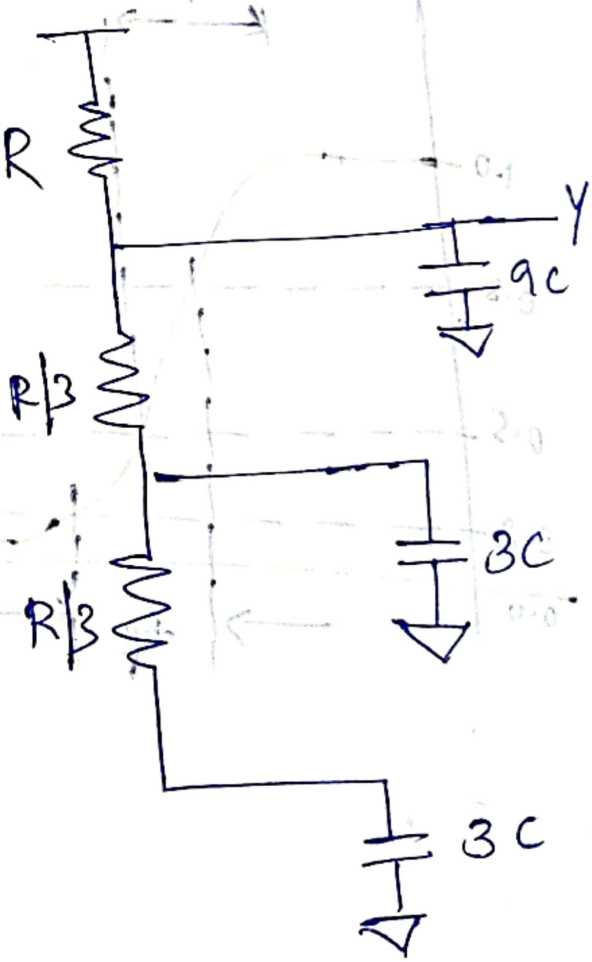




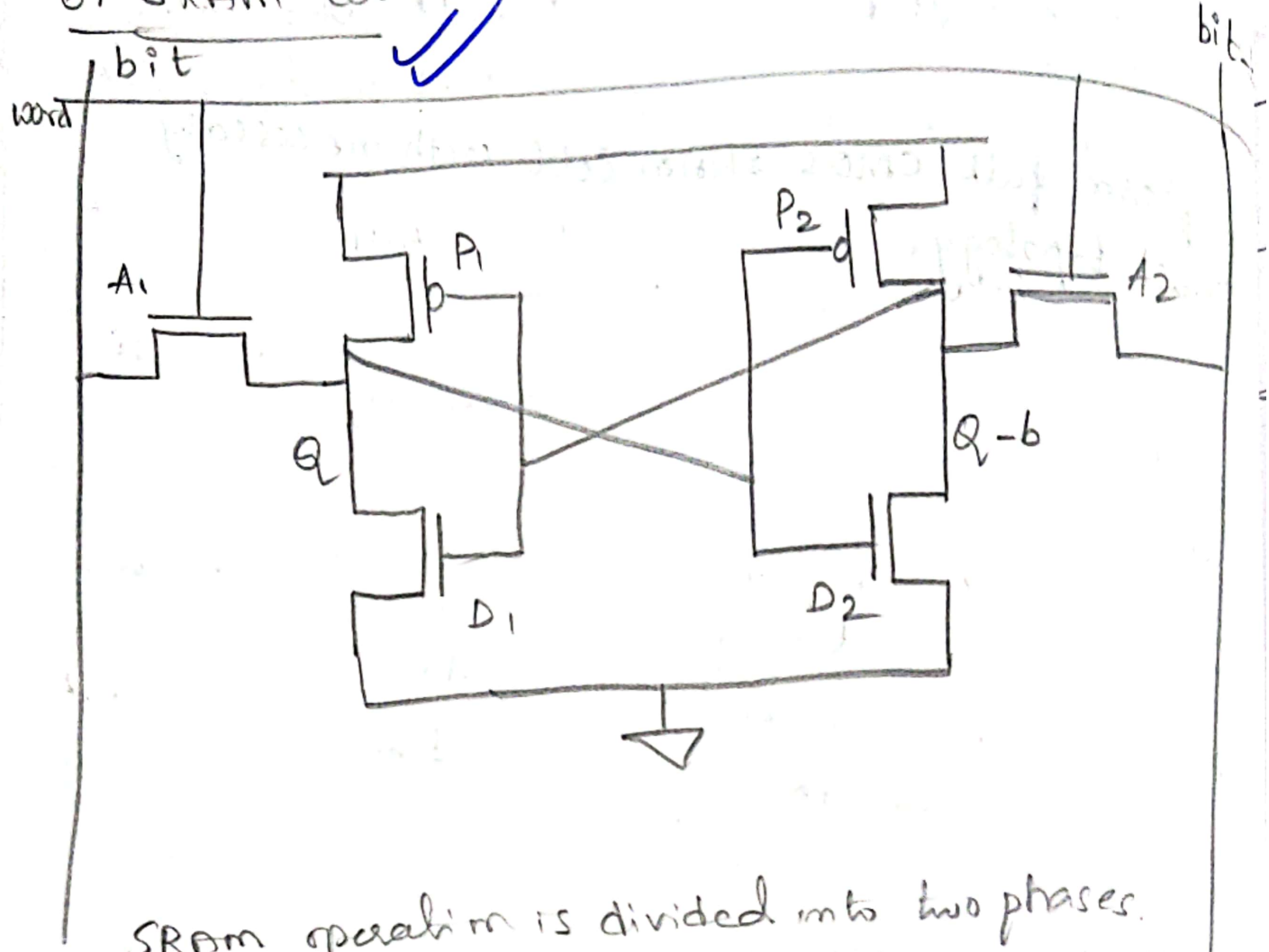
(iv) Falling



(v) Raising.



6T SRAM cell



SRAM operation is divided into two phases. The phases will be called ϕ_1 and ϕ_2, but may actually be generated from clk and its complement clkb.

Assume that in phase 2, the SRAM is precharged. In phase 1, the SRAM is read or written.

Read operation

→ SRAM cell being read.
→ The bitlines are both initially floating high.
→ Without loss of generality, assume Q is initially 0 and thus Q_b is initially 1.
→ Q_b and bit_b both should remain 1

→ When the word line is raised, bit should be pulled down through driver and access transistors D1 and A1.

At the same time bit is being pulled down, node Q tends to rise.

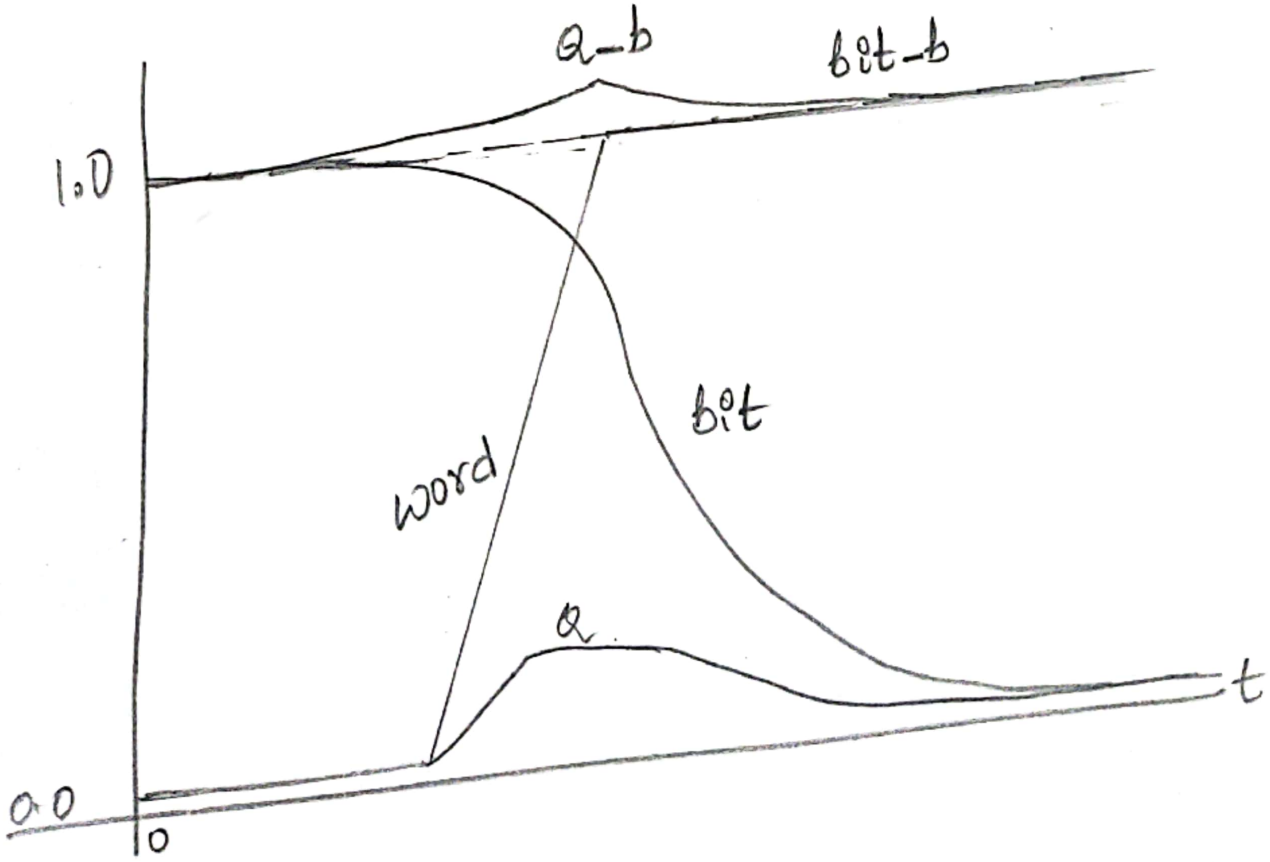
→ Q is held low by D1, but raised by current flowing in from A1.

→ Hence, the driver D1 must be stronger than the access transistor A1.

→ The transistors must be ratioed such that node Q remains below the switching threshold of the P2/D2 inverter.

→ This constraint is called read stability.

→ Observe that Q momentarily rises, but does not glitch badly enough to flip the cell.



Write operation

→ SRAM cell being written

→ Again, assume Q is initially 0 and that to write a 1 into the cell.

→ Bit is precharged high and left floating.

→ bit-b is pulled low by a write driver.

→ The read stability constraint that bit will be unable to force Q high through A1.

→ Hence, the cell must be written by forcing Q-b low through A2.

→ P_2 opposes this operation; thus, P_2 must be weaker than A2 so that Q-b can be pulled low enough.

→ This constraint is called writability.

→ Once Q-b falls low, D1 turns OFF and P1 turns ON, pulling Q high as desired.