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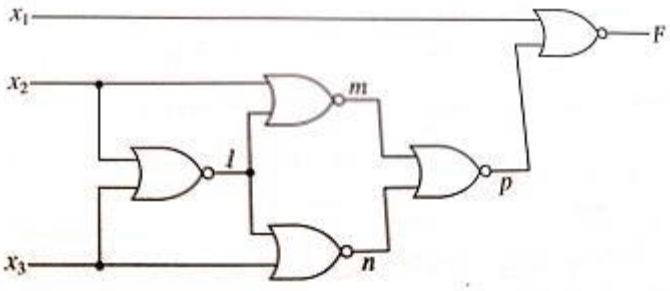
CMR INSTITUTE OF TECHNOLOGY

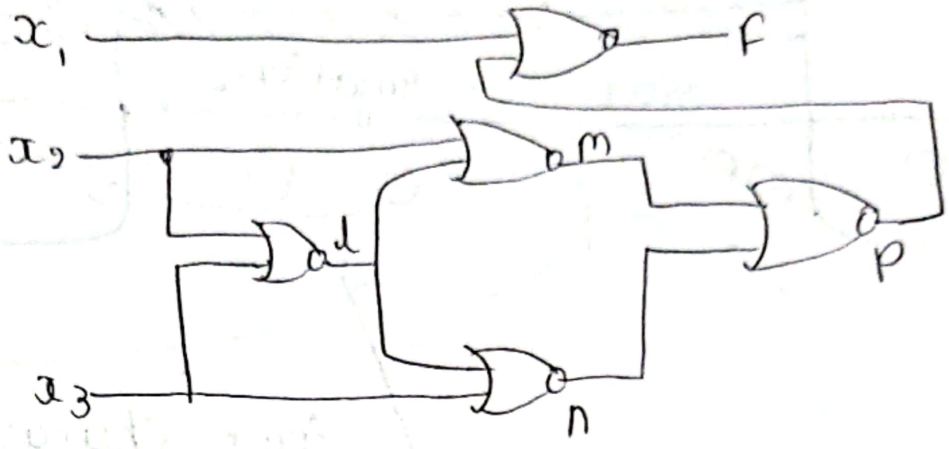
Internal Assesment Test – III									
Sub:	**VLSI DESIGN & TESTING**							**Code:**	**21EC63**
Date:	**29.07.2024**	**Duration:**	**90 mins**	**Max Marks:**	**50**	**Sem**	**VI**	**Branch**	**ECE-A,B,C,D**

Answer Any Five Questions

	Questions	Marks	OBE	
			CO	RBT
1.	Differentiate between fault and failure with an example. Explain different types of stuck at faults with example.	[10]	CO4	L2
2.	For the circuit shown in Fig.2 using Boolean difference (i) detect s@0 and s@1 at x2, (ii) determine partial Boolean difference for x2-l-n-p-F. 	[10]	CO4	L3
3.	What is fault diagnosis? Explain one dimensional path sensitization technique for combinational circuits with an example.	[10]	CO4	L2
4.	For the state table shown in Table, find (i) Response for 101 sequence, (ii) Homing tree, (iii) Distinguishing tree. **Present state** | **Input** $x=0$ $x=1$ A | B,0 D,0 B | A,0 B,0 C | D,1 A,0 D | D,1 C,0	[10]	CO5	L3
5.	With a neat logic diagram, explain clocked hazard free latches used in LSSD Technique.	[10]	CO5	L2
6.	Explain any two Adhoc design rules for improving testability.	[10]	CO5	L1

CI **CCI** **HOD**

2)



(i) $\frac{df(x)}{dx_i}$

$= \frac{df(x_1, x_2, x_1 \dots x_n)}{dx_i}$

$= f(x_1, \dots x_i \dots x_n) \oplus f(x_1, \dots \overline{x_i} \dots$

$= \frac{df}{dx_2} = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 x_3$

$f = \bar{x}_1 \bar{x}_3 + \bar{x}_1 x_3$

S @ 0 at $x = 2$, 010 @ 011

S @ 1 at $x = 2$, 000 @ 001

(ii) $\frac{df}{dx_2} = \frac{df}{dp} \cdot \frac{dp}{dn} \cdot \frac{dn}{dl} \cdot \frac{dl}{x_2}$

$\frac{df}{dp} = \frac{d}{dp}(\bar{x}_1 . p) = \bar{x}_1$

$\frac{dp}{dn} = \frac{d}{dn}(\bar{m} . \bar{n}) = \bar{m} = x_2 + \bar{x}_2 \bar{x}_3$

$$\frac{dn}{dx_1} = \frac{d}{dx_1}(x_1 \cdot \bar{x}_3) = \bar{x}_3$$

$$\frac{dy}{dx_2} = \frac{d}{x_2}(\bar{x}_2 \bar{x}_3) = \bar{x}_3$$

$$\frac{dF}{dx_2} = \bar{x}_1 \cdot x_2 + \bar{x}_2 \bar{x}_3 \cdot \bar{x}_3 \bar{x}_3$$

$$= \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 \bar{x}_2 \bar{x}_3$$

$\bar{x}_1 x_2 \bar{x}_3 = 011$

$\bar{x}_1 \bar{x}_2 \bar{x}_3 = 000$

4)

Present State	Input $x=0, x=1$	
A	B, 0	D, 0
B	A, 0	B, 0
C	D=1	A, 0
D	D=1	C, 0

(i) Response for 101 Sequence

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Initial	Input sequence	Output sequence	final sequence
A		001	C
B		100	A
C		101	B
D		010	C

(ii) Homing tree

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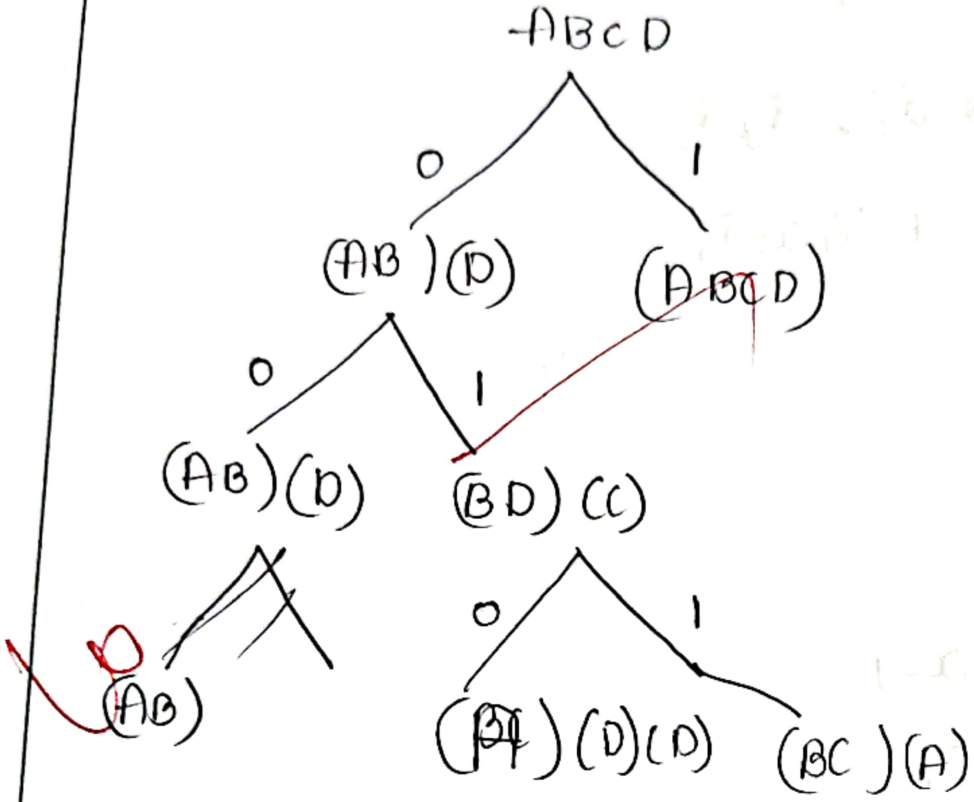

(iii) Distenguishing tree.

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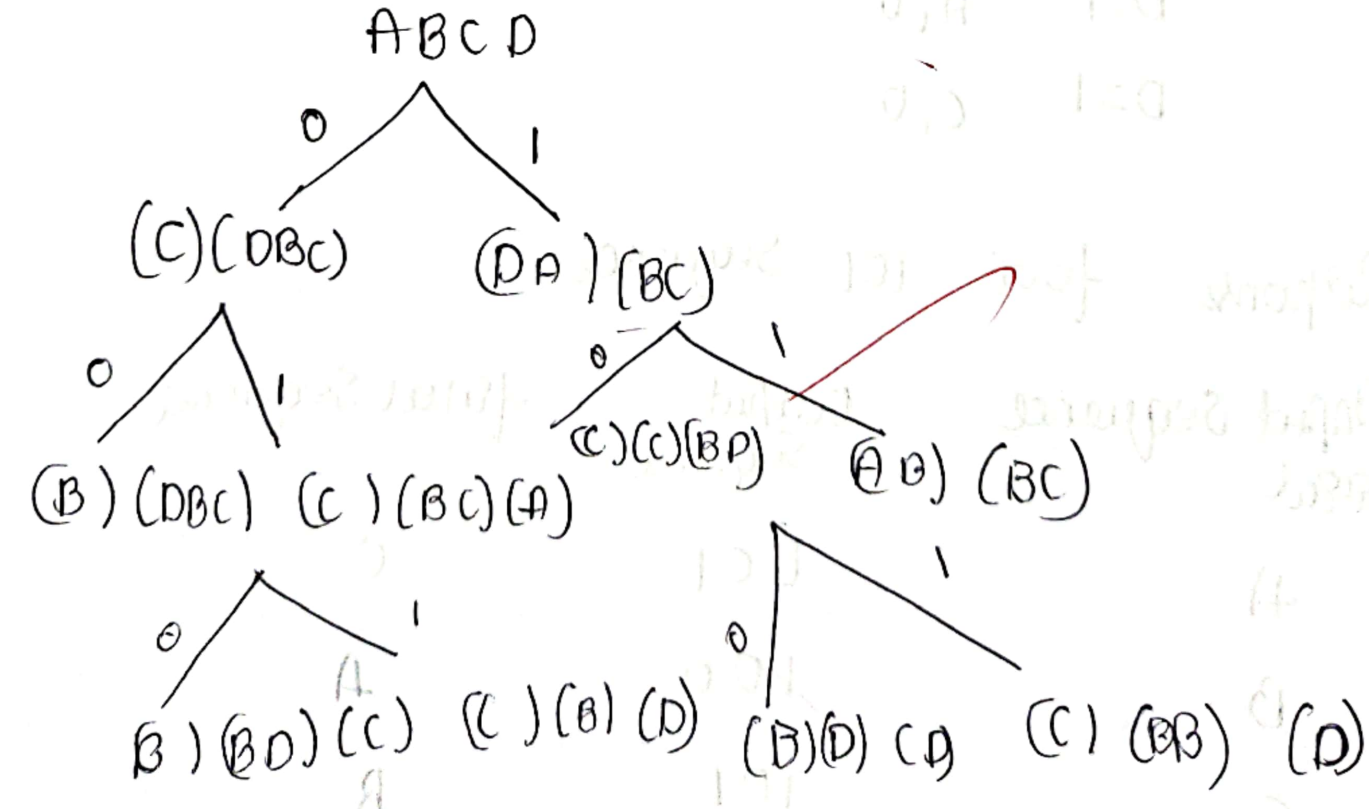
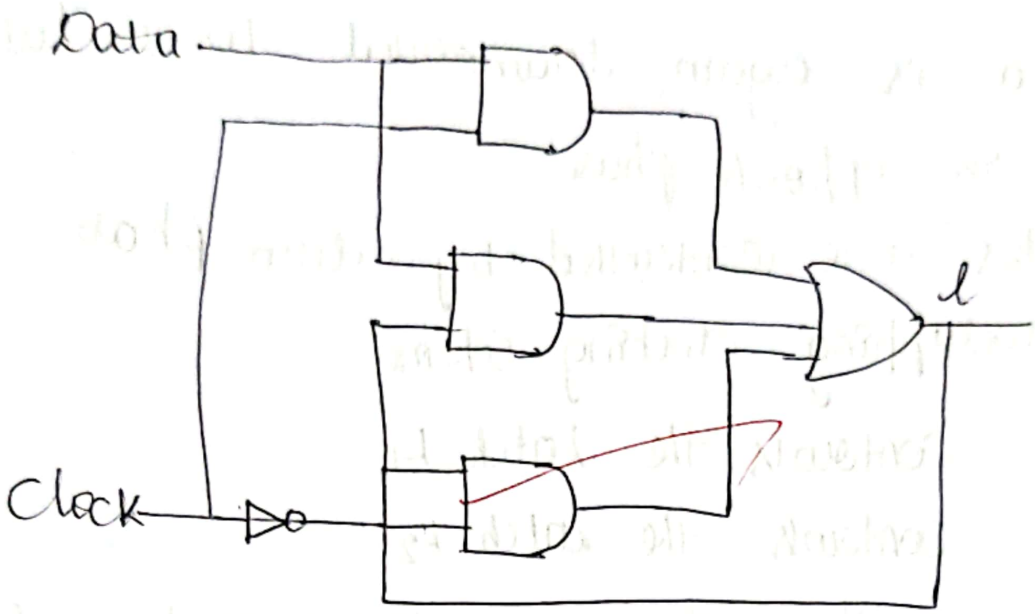


5)



AB \ CD	00	01	10	11	l
A0	A	A	B	A	0
B1	B	B	B	A	1

AB \ CD	00	01	10	11	l
0	0	0	1	0	0
1	1	1	1	0	1

* It has 2 inputs Data and the clock.
* If the clock, $C_1 = 0$, then it cannot change the state.
* If the clock, $C_1 = 1$, the internal state takes the value of the D input
* the LSSD employs two latches L_1 and

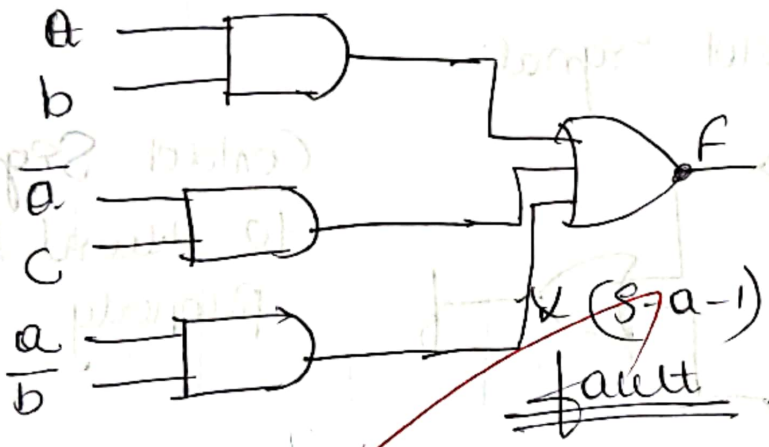
* The Data is captured into the Latch L_1 during the phase one
* the data is again transmitted to L_2 Latch during on opposite phase
* The latches are controlled by two phase non-overlapping clocking scheme
* phase 1 - controls the Latch L_1.
  phase 2 - controls the Latch L_2
* Data flow :- The data is transmitted to Latch one L_1 in phase 1 and again transmitted to Latch L_2 in phase 2.
* Hazard prevention :-
  1) Sequential Circuit
  2) Stable Storage

1) Sequential Circuit :- the non-overlaping clock scheme should ensure that only one latch should be active at one time
2) Stable Storage - during one clock cycle phase the inactive Latch should have previous stable state.

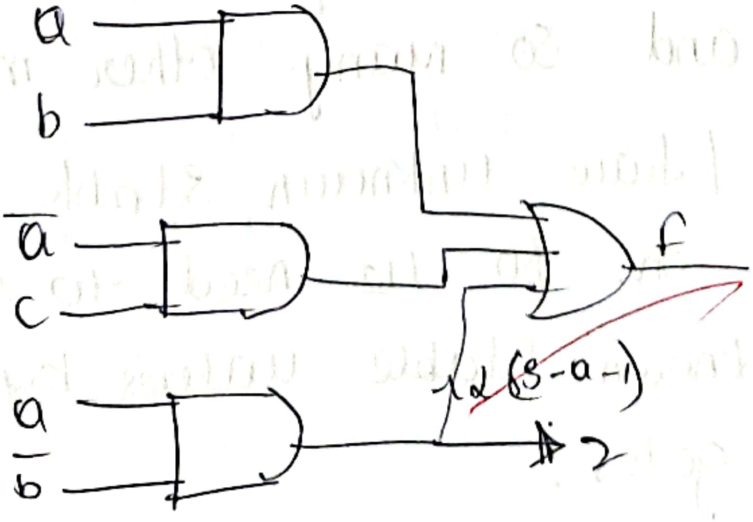
Benefits :- * Enhanced reliability
* Improved stability
* Reduced test complexity.

6) Two Adhoc design rules :-

1) Incorporate additional observation and control points in the circuit.

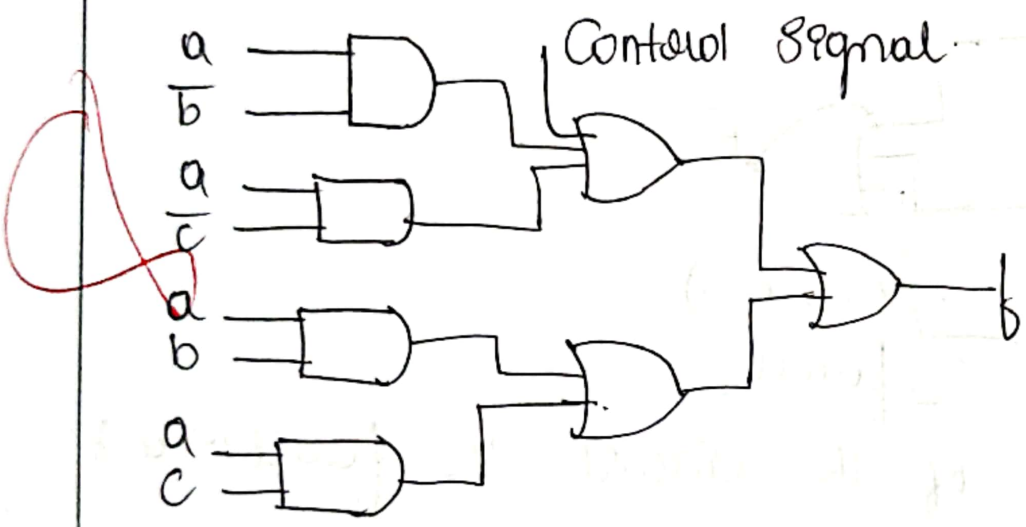


at the output of the circuit the fault (S-a-1) is not detectable.



If we add an extra output then, the fault (s-a-1) is detectable.

As we know, Nor gate output is always 0 hence the we get is very difficult to see the gate is working / functioning properly so adding extra control signal will make the Nor gate to work properly.



Control Signal to make Nor properly.

2) Circuit Initialization :- The flip flops, adders and the counters and so many other memory devices will show / have unknown stable values when the power is on. So we need to set the values into known stable values by an extra circuit & gates.

3. Fault diagnosis in digital circuits is the process of identifying and locating faults within the circuit. faults can occur due to various reasons, such as manufacturing defects, wear and tear. (or) Environmental factors.

One dimensional path sensitization - It is the method used in the testing of combinational circuits to detect faults.

Steps :-

1) Identify the fault :- Such as the stuck-at-0 (or) Stuck-at-1

2) Sensitize the fault - It involves finding an input combination that propagates the effect of the fault through the circuit to an observable output

3) Propagate the fault

4) Observe the output.

Example :-

$$Y = A \cdot B + \overline{C}.$$

Consider a simple combinational circuit with three inputs (A, B, C) and one output (y).

1) Identify the fault

Let us assume a Stuck-at-0 fault on input

2) Sensitize the fault :- We need to find an input combination, where the output y depends on B.

$Y = A \cdot B + \overline{C}$, if $C = 1$, $\overline{C} = 0$

Hence $Y = A \cdot B$.

Y directly depends on B

3) Propagating the fault -

Setting the inputs $A = 1$ and $C = 1$.

Output $Y = B$

If B is stuck-at-0, Y should be

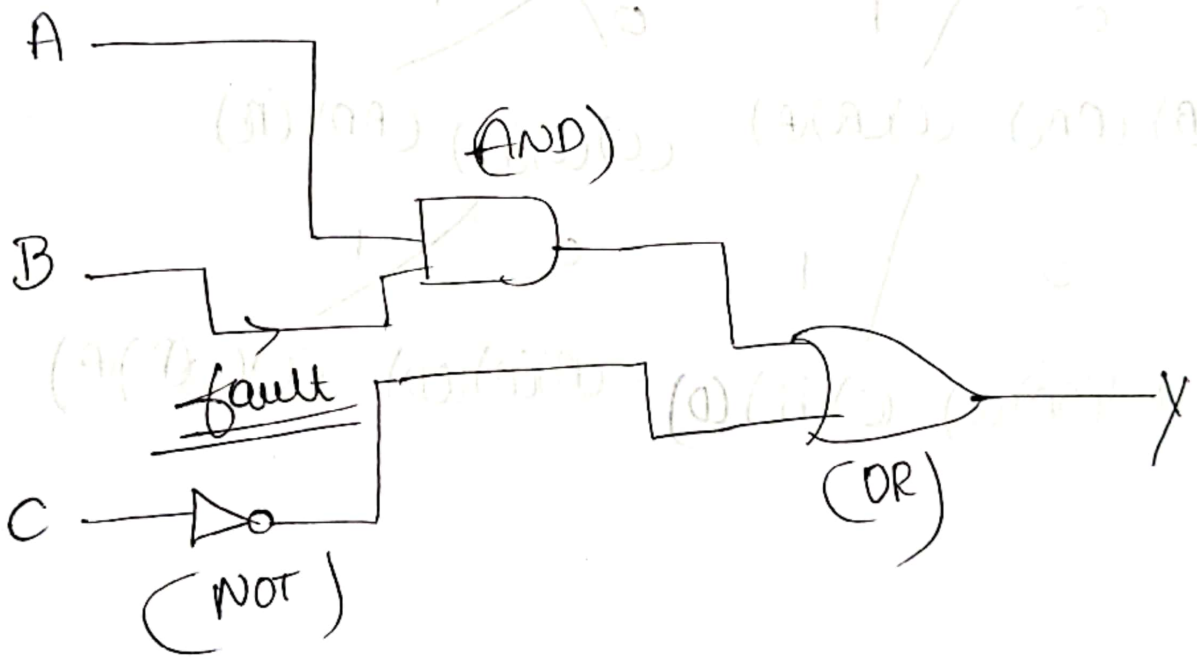
0, regardless of actual input B.

4) Observing the output -

If A=1, B=1, C=1

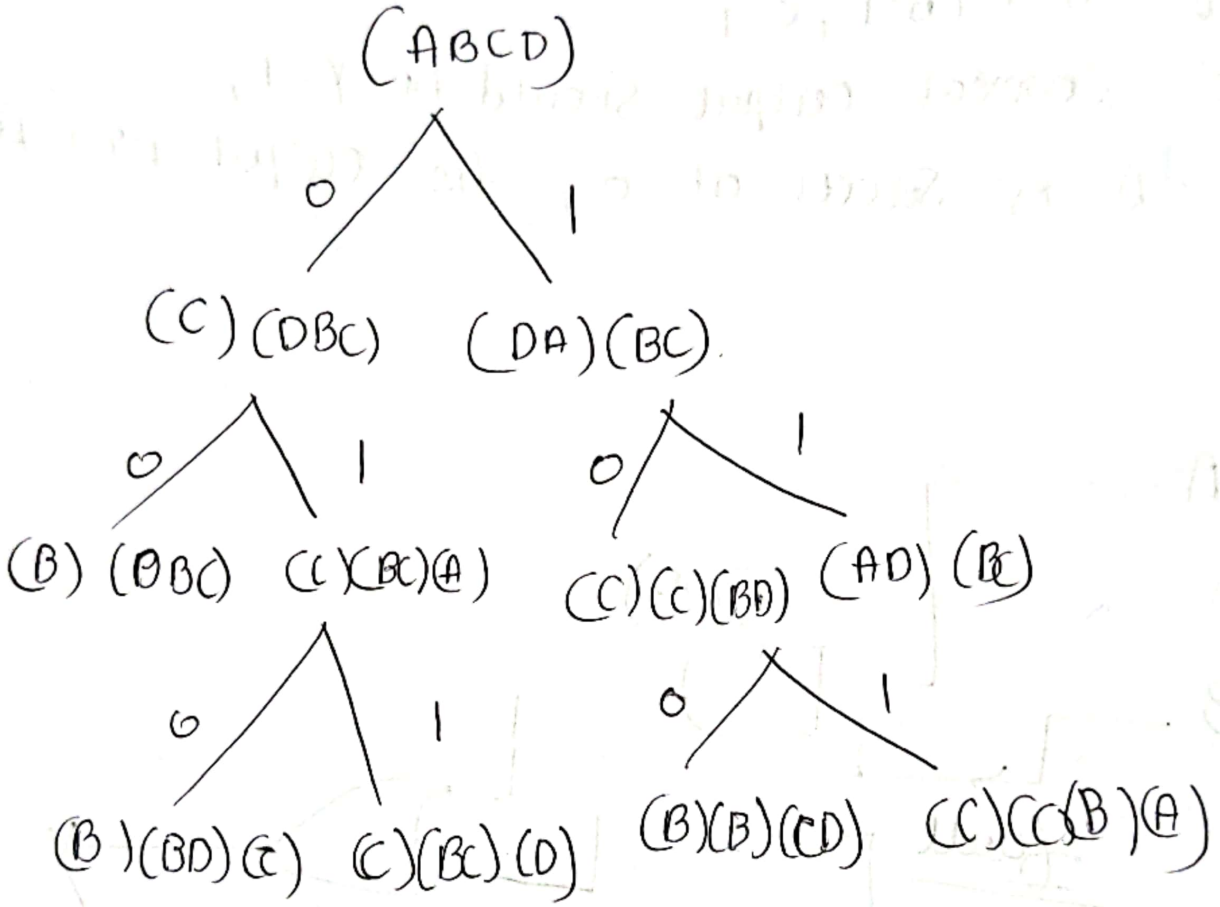
The correct output should be Y=1,

If B is Stuck-at-0, the output will be Y=0



4)

iii) Distinguishing tree



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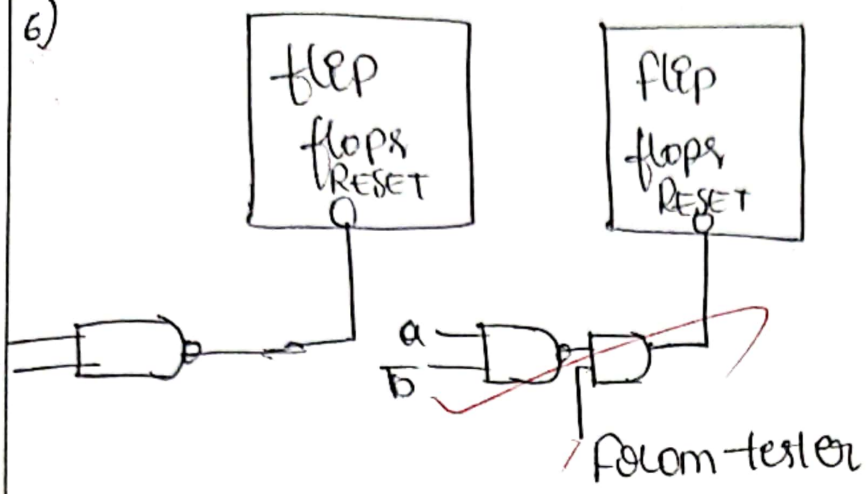

* All the circuits will have some faults in them.
* The fault may be detected or it may be undetectable.
* CMOS - Complementary Metal Oxide Semiconductor
* Incorporate additional observation and control points in the circuit
* If the additional observation and control points are not initialized the fault may not be detected
* If we add an extra output then the fault may be detected at the output.
* extra output line plays a very important role detecting the fault.