USN No. | | | | | | | | | | |

Internal Assessment Test 2– Dec 2024

Sub:	**Digital Design and Computer Organization**					Sub Code:	BCS302	Branch:	ISE	
Date:	13-12-2024	Duration:	90 min's	Max Marks:	50	Sem / Sec:	03/ A,B,C			OBE

	Answer any FIVE FULL QUESTIONS	MARKS	CO	RBT
1	a. Define bus arbitration. Explain in detail the approaches of bus arbitration. b. Show with diagram the memory hierarchy with respect to speed, size and cost	5+5	CO4	L2
2	What is DMA? Explain the hardware registers that are required in a DMA controller chip.Explain the use of DMA controller in a computer system with a neat diagram	10	CO4	L2
3	Explain different mapping functions used in cache memory.	10	CO4	L2
4	Explain with need diagram a single-bus structure connecting the memory to the processor	10	CO5	L2
5	Explain a complete processor execution with a neat diagram	10	CO5	L2
6	a.Explain the role of cache memory in pipelining. b.Explain the pipelining performance.	5+5	CO5	L2

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Internal Assessment Test 2 – Dec 2024
Scheme of Evaluation and Solution

Sub:	Digital Design and Computer Organization					Sub Code:	BCS302	Branch:	ISE
Date:	13.12.2024	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III A, B & C		OBE

Answer any FIVE FULL Questions	MARKS	CO	RBT
1.a. Define bus arbitration. Explain in detail the approaches of bus arbitration. **Bus Arbitration (2 marks)** Bus arbitration is a mechanism used to manage and coordinate multiple devices' access to a shared bus system in a computer. When multiple devices simultaneously request bus access, the arbitration mechanism determines which device gets priority and control of the bus. (2M) **Approaches to Bus Arbitration: (3M -1M Each)** **1. Daisy Chain Arbitration:** • Devices are connected in a serial chain • Bus request signal passes through each device sequentially • Priority is determined by physical position in chain • Advantages: Simple implementation, low cost • Disadvantages: Unfair to devices at end of chain, propagation delay **2. Centralized Parallel Arbitration:** • Uses a central arbitration unit • Each device has dedicated request and grant lines • Priority encoder determines access based on fixed or rotating schemes • Advantages: Faster than daisy chain, more flexible • Disadvantages: More complex wiring, higher cost **3. Distributed Arbitration:** • Devices determine priority through self-selection • Each device has unique ID number • Devices simultaneously place IDs on bus • Highest/lowest ID wins (depending on implementation) • Advantages: Fair access, no central controller needed • Disadvantages: Complex implementation	5	CO4	L2
1.b. Show with diagram the memory hierarchy with respect to speed , size and cost **Diagram of Memory Hierarchy:(2M)** **Key Characteristics of Memory Hierarchy(3M)** **1. Registers:** • Fastest access (< 1ns) • Very small capacity (bytes) • Highest cost per bit • Located in CPU 2. **Cache Memory**: • Fast access (1-10ns) • Small capacity (KB to MB) • High cost per bit • Located between CPU and main memory **3. Main Memory (RAM):** • Medium access speed (50-100ns) • Medium capacity (GB) • Moderate cost per bit • Primary storage for active programs **4. Secondary Storage:** • Slow access (ms) • Large capacity (TB) • Lowest cost per bit • Permanent storage	5	CO4	L2
2. What is DMA? Explain the hardware registers that are required in a DMA controller chip. Explain the use of DMA controller in a computer system with a neat diagram **Defintion of DMA(2M)** DMA is a feature that allows certain hardware subsystems within a computer to access main system memory independently of the CPU. This enables data transfer between I/O devices and memory without continuous CPU intervention.	10	CO4	L2

Diagram (2M) **Required Hardware Registers in DMA Controller: (3M)** 1. Memory Address Register (MAR): • Holds the starting address for memory transfer • Updated after each transfer • Specifies source/destination in memory 2. Byte Count Register: • Contains number of bytes to be transferred • Decremented after each transfer • Transfer stops when count reaches zero 3. Control Register: • Contains control bits: o Read/Write control o Transfer mode selection o Interrupt enable/disable o Status flags o Operating mode bits 4. Status Register: • Indicates: o Transfer completion o Error conditions o Device status o Ready/busy status **DMA Operation: (3M)** 1. CPU initiates DMA transfer 2. DMA controller takes control of system bus 3. Transfer occurs directly between memory and I/O device 4. DMA controller signals completion to CPU 5. CPU resumes normal operation			
3. Explain different mapping functions used in cache memory. **Definition of Cache Mapping Functions (1M)** There are three main mapping functions used in cache memory: **1. Direct Mapping: (3M)** • Simplest mapping technique • Each memory block mapped to only one cache line • Mapping formula: i = j modulo m where i = cache line number j = memory block number m = number of lines in cache • Advantages: Simple implementation, low hardware cost • Disadvantages: Higher conflict miss rate **2. Associative Mapping (Fully Associative): (3M)** • Memory block can be mapped to any cache line • Content Addressable Memory (CAM) used for tag comparison • All tags compared simultaneously • Advantages: Most flexible, lowest miss rate • Disadvantages: Complex hardware, expensive, slower comparison 3. **Set-Associative Mapping**: (3M) • Compromise between direct and associative mapping • Cache divided into sets, each with multiple lines • Memory block maps to specific set but can be placed anywhere within set • n-way set associative: n lines per set • Mapping formula: Set number = (Memory block address) modulo (Number of sets) • Common implementations: 2-way, 4-way, 8-way • Best balance of hardware complexity and hit rate	10	CO4	L2
4.Explain with need diagram a single-bus structure connecting the memory to the processor **Introduction and Overview of** Single Bus **(2 marks):** • Definition of a datapath and its purpose. • Role of the datapath in facilitating communication between the processor and memory. **Components of the Datapath (4 marks):** • Processor Registers (1 mark): o Role of registers (e.g., MAR, MDR) in memory communication. • Address Bus (1 mark): o Used to specify memory locations. o Unidirectional flow from processor to memory. • Data Bus (1 mark):	10	CO5	L2

○ Transfers data between the processor and memory. ○ Bidirectional flow. • Control Signals (1 mark): ○ Read/write control signals for memory operations. **Step-by-Step Operation (1 marks):** • **Addressing** ○ How the processor generates a memory address and sends it via the address bus. • **Data Transfer** ○ Memory read: Memory sends data to the processor via the data bus. ○ Memory write: Processor sends data to memory. • **Synchronization** ○ Role of control signals (e.g., memory enable, write enable) in coordinating actions. **Diagram (3Mark)**			
5.Explain a complete processor execution with a neat diagram **Instruction Execution Cycle:** **Instruction Fetch (IF): (1 Mark)** PC contents transferred to MAR Memory read signal activated Instruction loaded into MBR Instruction transferred to IR Program Counter incremented **Instruction Decode (ID): (1 Mark)** Opcode extraction from IR Operand address calculation Source operand fetch from registers Control signal generation Hazard detection **Operand Fetch: For Register Operands: (1 Mark)** Read from register file Values placed in temporary registers **For Memory Operands: (1 Mark)** Address calculation Memory access initiated Data loaded into MDR Transfer to ALU registers Execution (EX): ALU performs operation based on opcode For arithmetic: Addition, subtraction, etc. For logical: AND, OR, XOR, etc. For shift: Left/right shifts Condition codes set (Zero, Carry, etc.) Memory Access (MEM) if needed: Address computation complete Memory read/write signals activated Data transfer between memory and registers Cache checking and updating **Write Back (WB): (1 Mark)** Results written to destination register Status flags updated Memory updated if store instruction PC updated for branch instructions Control Unit Operations: Generates all control signals Coordinates timing between stages Manages pipeline flow Handles interrupts and exceptions **Example of ADD R1, R2, R3: (3Marks)** Fetch ADD instruction Decode: Identify ADD operation Read R2, R3 values Execute: R2 + R3 Write result to R1 **Diagram-2Marks**	10	CO5	L2

6. a. Explain the role of cache memory in pipelining. **b. Explain pipelining performance.** **Introduction and Definition (2 marks):** • Definition of pipeline hazards. • Mention of their importance in instruction pipelining. **Types of Pipeline Hazards (6 marks):** • Structural Hazards (2 mark): o Resource conflicts explained with an example. • Data Hazards (2 marks): o Explanation and types (RAW, WAR, WAW). o Mitigation techniques like forwarding or stalling. • Control Hazards (2 mark): o Impact of branch instructions on the pipeline and strategies like branch prediction. **Mitigation Techniques (2 marks):** • Explanation of general methods to resolve pipeline hazards, including examples: o Hardware duplication for structural hazards. o Data forwarding or stalling for data hazards. o Branch prediction for control hazards.	10	CO5	L2

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