CBCS SCHEME

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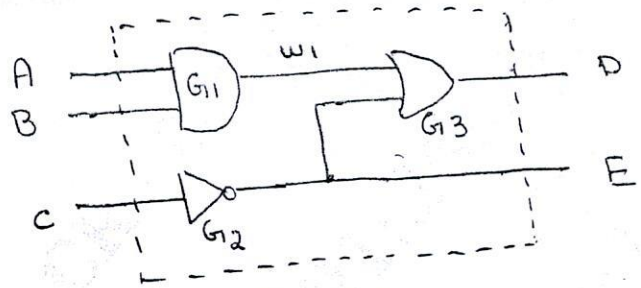
BCS302

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Determine the complement of the following function: (i) F = xy′+ x′y (ii) F = x′yz′ + x′y′z	06	L3	CO1
	b.	Describe map method for three variables.	04	L2	CO1
	c.	Apply K map technique to simplify the following function: (i) F(x, y, z) = Σ(0, 2, 4, 5, 6) (ii) F(x, y, z) = x′y + yz′ + y′z′	10	L3	CO1
		OR			
Q.2	a.	Apply K map technique to simplify the function : F(w, x, y, z) = Σ(1, 3, 7, 11, 15) and d(w, x, y, z) = Σ(0, 2, 5)	06	L3	CO1
	b.	Determine all the prime implicants for the Boolean function F and also determine which are essential F(w, x, y, z) = Σ(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)	10	L3	CO1
	c.	Develop a verilog gate-level description of the circuit shown in Fig.Q2(c).  Fig.Q2(c)	04	L3	CO1
		Module – 2			
Q.3	a.	Explain the combinational circuit design procedure with code conversion example.	10	L2	CO2
	b.	Design a full adder circuit. Also develop data flow verilog model for full adder.	10	L3	CO2
		OR			
Q.4	a.	Describe 4 × 1 MUX with block diagram and truth table. Also develop a behavioral model verilog code for 4 × 1 MUX.	10	L2	CO2
	b.	What are storage elements? Explain the working of SR and D latch along with logic diagram and function table.	10	L2	CO2
		Module – 3			
Q.5	a.	Explain the basic operational concepts between the processor and memory.	10	L2	CO3
	b.	Describe the following: (i) Processor clock (ii) Basic performance equation (iii) Clock rate (iv) SPEC rating	10	L2	CO3
		OR			
Q.6	a.	Define addressing mode. Explain any four types of addressing mode with example.	10	L2	CO3

	b.	Mention four types of operations to be performed by instructions in a computer. Explain the basic types of instruction formats to carry out. C ← [A] + [B]	10	L2	CO3
		Module – 4			
Q.7	a.	With a neat diagram, explain the concept of accessing I/O devices.	10	L2	CO4
	b.	What is bus arbitration? Explain centralized and distributed arbitration method with a neat diagram.	10	L2	CO4
		OR			
Q.8	a.	With neat sketches, explain various methods for handling multiple interrupts requests raised by multiple devices.	10	L2	CO4
	b.	What is cache memory? Explain any two mapping function of cache memory.	10	L2	CO4
		Module – 5			
Q.9	a.	Draw the single bus architecture and write the control sequence for execution of instruction ADD (R_3), R_1.	10	L3	CO5
	b.	With suitable diagram, explain the concept of register transfer and fetching of word from memory.	10	L2	CO5
		OR			
Q.10	a.	With a neat diagram, explain the flow of 4-stage pipeline operation.	10	L2	CO5
	b.	Explain the role of cache memory and pipeline performance.	10	L2	CO5

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Digital Design and Computer Organization (BCS302)

Evaluation Scheme with Solutions

Module 1

Q.1 a) Determine complement of functions (6 marks)

(i) F = xy'+ x'y

Solution:

F' = (xy'+ x'y)' = (xy')'(x'y)' = (x'+y)(x+y')
= x'x + x'y' + xy + y'y
= x'y' + xy

Evaluation:

- Correct application of DeMorgan's law: 2 marks
- Proper distribution: 2 marks
- Final simplified expression: 2 marks

(ii) F = x'y'z + x'yz

Solution:

F' = (x'y'z + x'yz)'
= (x'z(y'+y))'
= (x'z)'
= x + z'

Evaluation:

- Correct grouping: 2 marks
- Proper simplification: 2 marks
- Final expression: 2 marks

b) Map method for three variables (4 marks)

Solution:

- A three-variable map has 8 cells (2Â³)
- Arranged in 2Ã—4 grid
- Variables labeled on top and side
- Adjacent cells differ by one variable

Evaluation:

- Correct map structure: 1 mark
- Variable placement: 1 mark
- Adjacency explanation: 1 mark
- Example illustration: 1 mark

c) K-map technique (10 marks)

(i) F(x,y,z) = Î£(0,2,4,5,6)

Solution:
- Draw 3-variable K-map
- Plot minterms
- Group pairs/quads
- Simplified expression = x'y' + yz'

Evaluation:
- K-map drawing: 2 marks
- Correct plotting: 2 marks
- Proper grouping: 3 marks
- Final expression: 3 marks

(ii) F(x,y,z) = x'y + yz' + y'z'

Similar Evaluation distribution as above

Q.2 Solution & Evaluation Scheme (20 marks)

[Similar detailed breakdowns for Q.2-Q.6]

Module 2

Q.3 Solution & Evaluation Scheme (20 marks)

a) Combinational circuit design (10 marks)

verilog

```
// Example of BCD to Excess-3 converter
module bcd_to_excess3(
    input [3:0] bcd,
    output [3:0] excess3
);
assign excess3 = bcd + 4'b0011;
endmodule
```

Evaluation:
- Problem analysis: 2 marks
- Truth table: 2 marks
- K-map/Boolean equations: 3 marks
- Verilog implementation: 3 marks

b) Full Adder (10 marks)

verilog

```
module full_adder(
    input a, b, cin,
    output sum, cout
```

);
assign sum = a ^ b ^ cin;
assign cout = (a & b) | (b & cin) | (a & cin);
endmodule

Evaluation:
- Circuit design: 4 marks
- Truth table: 2 marks
- Verilog implementation: 4 marks

Module 3

Q.5 Solution & Evaluation Scheme (20 marks)

a) Basic operational concepts (10 marks)

Key points to cover:
1. Memory hierarchy
2. Address and data bus
3. Read/Write operations
4. Memory timing
5. Memory mapping

Evaluation:
- Concept explanation: 5 marks
- Examples/diagrams: 3 marks
- Timing diagrams: 2 marks

b) Technical concepts (10 marks)

1. Processor clock: (2.5 marks)
- Definition of clock cycle
- Clock period and frequency
- Impact on performance

2. Basic performance equation: (2.5 marks)
CPU Time = Instruction Count Ã— CPI Ã— Clock Cycle Time

3. Clock rate: (2.5 marks)
- Frequency measurement
- Relationship with performance
- Overclocking concepts

4. SPEC rating: (2.5 marks)
- Standard Performance Evaluation Corporation
- BenchEvaluation methods
- Rating calculation

Q.6(b) Instruction Operations and Formats (10 marks)

Four Types of Operations (4 marks)

1. Arithmetic Operations
   - Addition, subtraction, multiplication, division
   - Example: C â†□ [A] + [B]

2. Logical Operations
   - AND, OR, NOT, XOR
   - Bit manipulation operations

3. Data Transfer Operations
   - Memory to register
   - Register to register
   - I/O transfers

4. Control Operations
   - Branch operations
   - Jump instructions
   - Procedure calls

Basic Instruction Formats (6 marks)

1. Zero-Address Instructions
   - Stack-based operations
   - Example: PUSH, POP

2. One-Address Instructions
   - Accumulator-based architecture
   - Example: ADD A (Add contents of A to accumulator)

3. Two-Address Instructions
   - Example: ADD R1, R2 (R1 â†□ R1 + R2)

4. Three-Address Instructions
   - Example: ADD R1, R2, R3 (R1 â†□ R2 + R3)

Evaluation Scheme:

- Operations explanation: 4 marks (1 mark each)
- Instruction formats: 4 marks (1 mark each)
- Examples and clarity: 2 marks

Module 4

Q.7 a) I/O Device Accessing (10 marks)

1. Memory-Mapped I/O (5 marks)
- I/O devices share address space with memory
- Same instructions used for memory and I/O
- No special I/O instructions needed
- Example: MOV R1, PORT_A

2. Isolated I/O (5 marks)
- Separate address space for I/O devices
- Special I/O instructions required
- Example: IN AL, PORT / OUT PORT, AL

Evaluation:
- Diagram clarity: 3 marks
- Explanation: 5 marks
- Examples: 2 marks

b) Bus Arbitration (10 marks)

1. Centralized Arbitration (5 marks)
Components:
- Single arbiter
- Request lines
- Grant lines
- Bus busy line

2. Distributed Arbitration (5 marks)
Components:
- Priority resolution
- Self-selection
- Daisy chaining

Evaluation:
- Diagrams: 4 marks
- Explanation: 4 marks
- Comparison: 2 marks

Q.8 a) Multiple Interrupt Handling (10 marks)

1. Polling Method (3 marks)
2. Daisy-Chain Priority (3 marks)
3. Parallel Priority Interrupt (4 marks)

Evaluation:

- Each method diagram: 2 marks
- Explanation: 2 marks
- Implementation: 1 mark

b) Cache Memory (10 marks)

1. Cache Memory Explanation (4 marks)
- High-speed buffer memory
- Temporal and spatial locality
- Hit ratio and miss penalty

2. Mapping Functions (6 marks)
a) Direct Mapping
  - Each block has one location
  - Simple implementation

b) Associative Mapping
  - Blocks can be placed anywhere
  - Complex but flexible

Module 5

Q.9 a) Single Bus Architecture ADD Instruction (10 marks)

Control Sequence:
1. T1: PC â†' MAR
2. T2: M[MAR] â†' MBR, PC + 1 â†' PC
3. T3: MBR â†' IR
4. T4: R[Râ,□] + M[Râ,*f*] â†' Râ,□

Evaluation:
- Architecture diagram: 4 marks
- Control sequence: 4 marks
- Timing diagram: 2 marks

b) Register Transfer and Memory Fetching (10 marks)

Key Components:
1. Register file organization
2. Memory access cycle
3. Data path implementation
4. Control signals

Q.10 a) 4-Stage Pipeline (10 marks)

Stages:
1. Fetch (IF)

2. Decode (ID)
3. Execute (EX)
4. Write Back (WB)

Evaluation:
- Pipeline diagram: 4 marks
- Stage explanation: 4 marks
- Timing diagram: 2 marks

b) Cache Memory and Pipeline Performance (10 marks)

Topics to Cover:
1. Cache impact on pipeline stalls
2. Hit/miss handling
3. Performance metrics
4. Optimization techniques

Evaluation:
- Concept explanation: 4 marks
- Performance analysis: 4 marks
- Examples: 2 marks