CBCS SCHEME

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21EC71

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Advanced VLSI

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain ASIC design flow with neat flow chart. **(10 Marks)**

b. Explain Booth Encoding multiplier with an example. **(10 Marks)**

OR

2 a. Describe different cell compilers and I/O cells. **(10 Marks)**

b. With a neat diagram, explain the operation of conditional sum adder. Mention its advantages and disadvantages. **(10 Marks)**

Module-2

3 a. Explain the concept of measurement of delay in Floorplanning. **(10 Marks)**

b. Explain the following :
i) Power planning ii) Clock planning **(10 Marks)**

OR

4 a. Write an algorithm for iterative placement improvement method and explain briefly. **(10 Marks)**

c. Explain the goals and objectives of global routing in detail. **(10 Marks)**

Module-3

5 a. Explain factors in randomizing the stimulus to a design. **(10 Marks)**

b. Draw the diagram of layered test bench of system verilog and describe the function of each layer. **(10 Marks)**

OR

6 a. Describe the various array methods with an example. **(08 Marks)**

b. Describe type def and enumerated data types with example. **(06 Marks)**

c. Explain constant and strings in system verilog with example. **(06 Marks)**

Module-4

7 a. Explain Tasks, functions and void function in system verilog. **(06 Marks)**

b. How time values are specified in system verilog, describe with example. **(06 Marks)**

c. Explain automatic storage and variable initialization with system verilog program example. **(08 Marks)**

OR

8 a. Describe the communication between the test bench and DUT with suitable diagram and system verilog program. **(10 Marks)**

b. Explain different types of system verilog assertions with example. **(10 Marks)**

Module-5

9 a. Explain common randomization problems in brief. (10 Marks)
b. Write any 4 Random Number functions with an example. (04 Marks)
c. Explain Pseudorandom Number Generators (PRNG) in system verilog. (06 Marks)

OR

10 a. What is coverage? Explain coverage types in system verilog. (10 Marks)
b. Describe various coverage options with an example. (10 Marks)

* * * * *

1. Ans) > Application Specific Integrated Circuits (ASIC) are the ICs which are designed for a to perform specific function for particular application.

> They vary from other Integrated Circuits or IC in performing their logical functions.

> ASICs are made up of cells and metal-interconnects.

> A cell is an abstraction that performs various logical functions in the ASICs

> A metal interconnect is that which connects various cells together in the system.

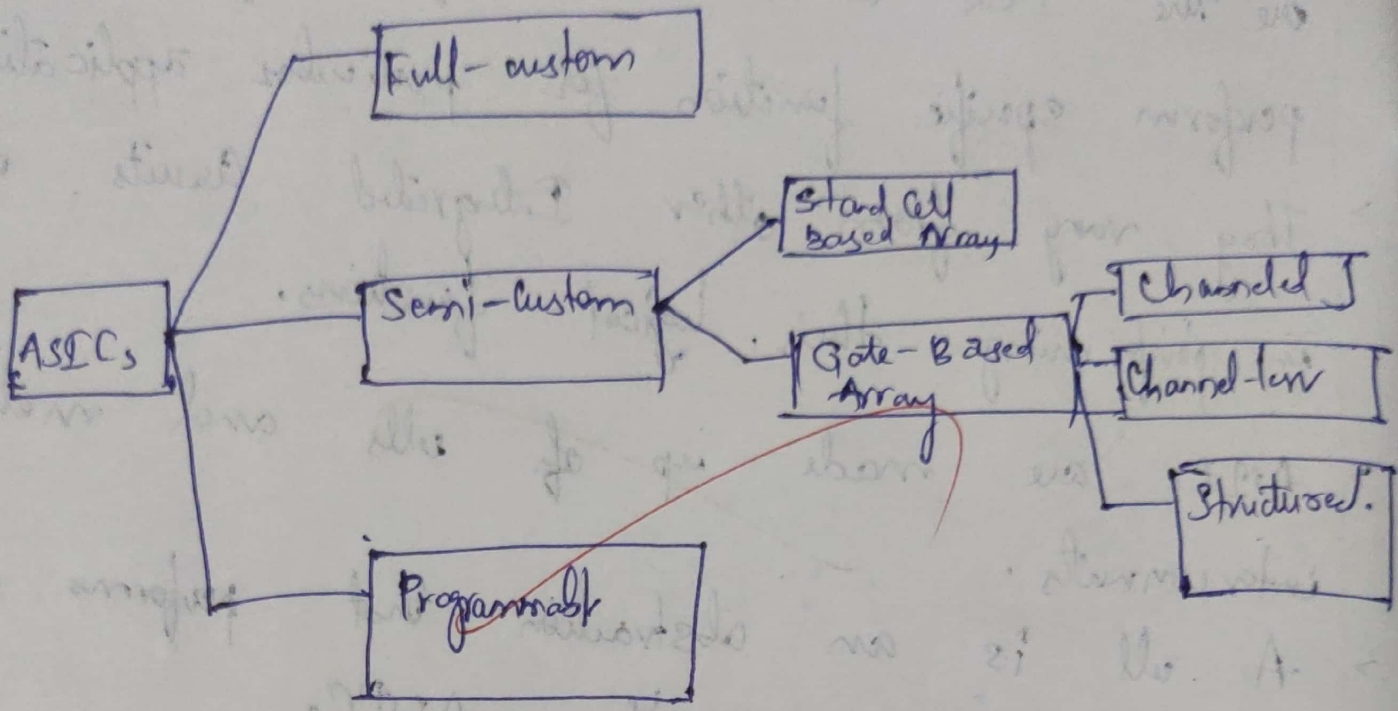
> Hence, architecture mainly consist of cells and metal inter-connects.

> ASICs are mainly classified into three categories

(i) Full-Custom

(ii) Semi-Custom

(iii) Programmable Logic Device.



(i) Full-Custom ASIC

- Full-custom ASICs are customised (pre-defined by the user) which performs the specific applications.
- The cannot be altered once their final finishing is done by the manufacturer.
- The has reduced area and reduced manufacturing cost as it cannot be altered every-time.
- These are having high level of accuracy in the system where they cannot be changed.

(ii) Semi-Custom IC

> Semi-custom ICs are such kind that can be altered by the cells and mask layers.

> They are pre-defined but can be customised according to the user or the system.

> Semi-custom IC mainly consist of two-types;

(A) Standard cell Based Array

(B) Gate Based Array.

> (A) Standard Cell Based Array

- Consists of the various layers of the cell which can be customised in the different manner according to the user.

> Standard cell Based Array can also be known as CBIC which does not make any variation in the components of the system.

> (B) Gate-Based Array

- Gate based array consists of a cells and where mask layers can be customised using silicon wafers.

→ Gate Based Array consists of 3 types:
- Channelless
- Channelled
- Structured.

(iii) Programmable Logic Devices

→ These are the special type of IC that are considered in the micro-electronic systems.

> The electronically RAM or EPROM can change its characteristics by applying the high voltage.

> EPROM also can change its characteristics by applying the UV light at high voltage.

→ These PLDs have special features which consists of macro and other layer of cells.

2. Ans) (A) Cell Based ASIC

> A standard cell based ASIC consists of various layers which can be modified or customised in different manner according to the user.

> Standard Cell Based array can also be known as CBIC which does not make any variation in the component of the system.

> The cells in the standard cell based array are known as full-custom macros or designable manner.

> It mainly consists of one central library and other four block.

> All the four block are interconnected through the metal inter-connects.

> The main advantage of cell-based ASIC are they can be designed easily with low cost.

- The main disadvantage of cell based ASIC is increased demand to its production in the systems.
- The designing can cost heavy in the system.

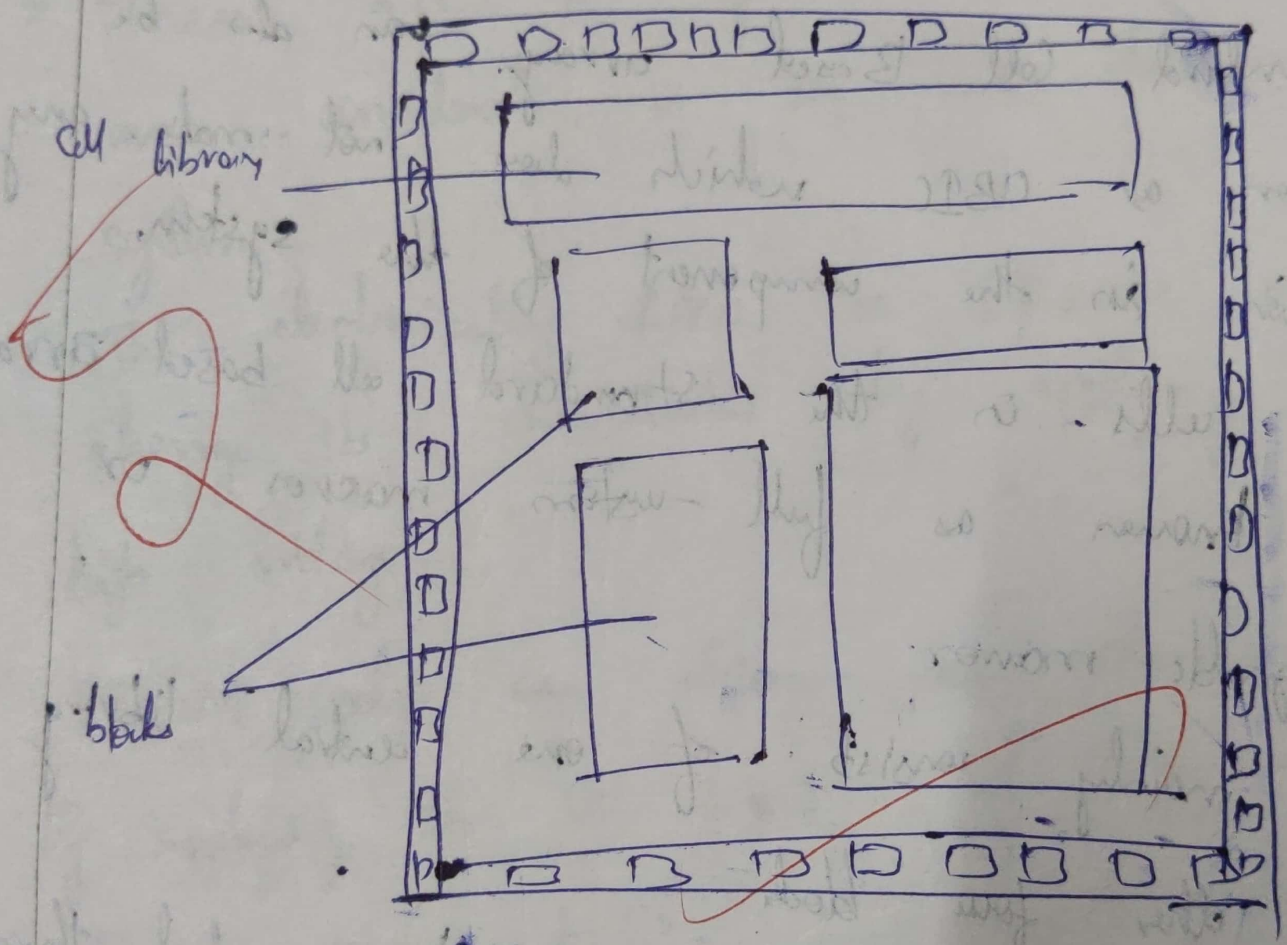


Fig: (a) Cell - Based ASIC

(B) Gate Array based ASIC

> Gate Array based ASIC is designed to perform the specific function for a particular application.

> The cells in Gate Array Based ASIC are called as MACROS.

> Gate Array based ASIC consists of three major types:

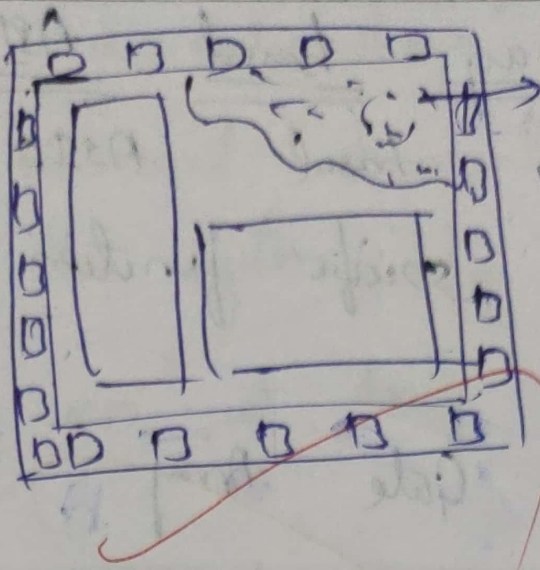
(i) Channelless

(ii) Channelled

(iii) Structured.

> (i) Channelless

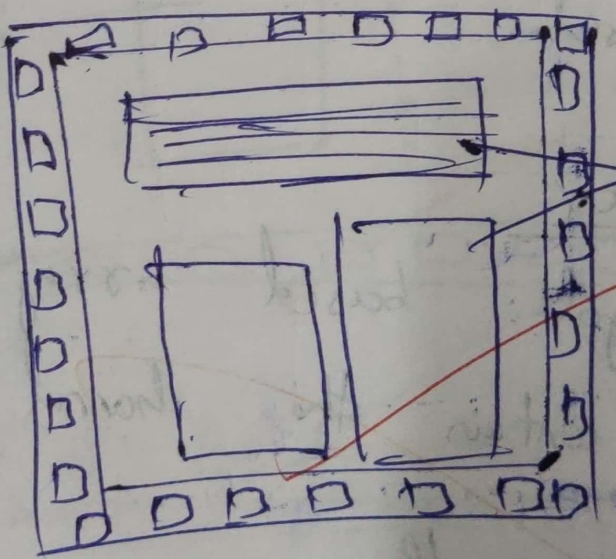
- Channelless gate based array such which do not contain the channel at any of the system in the area.



(ii) Channelled

> The gate based ASICs are the systems that will be customised using the silicon wafer in the system.

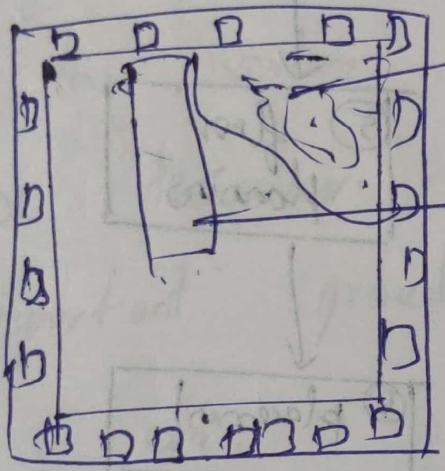
> These will be channel according to the requirement of the user.



(iii) Structured

> A structured gate based array is the system that will perform specific functions in the system.

> Consists of cells and mask layers is ngsar where only mask layers can be customised in the system.



Advantages

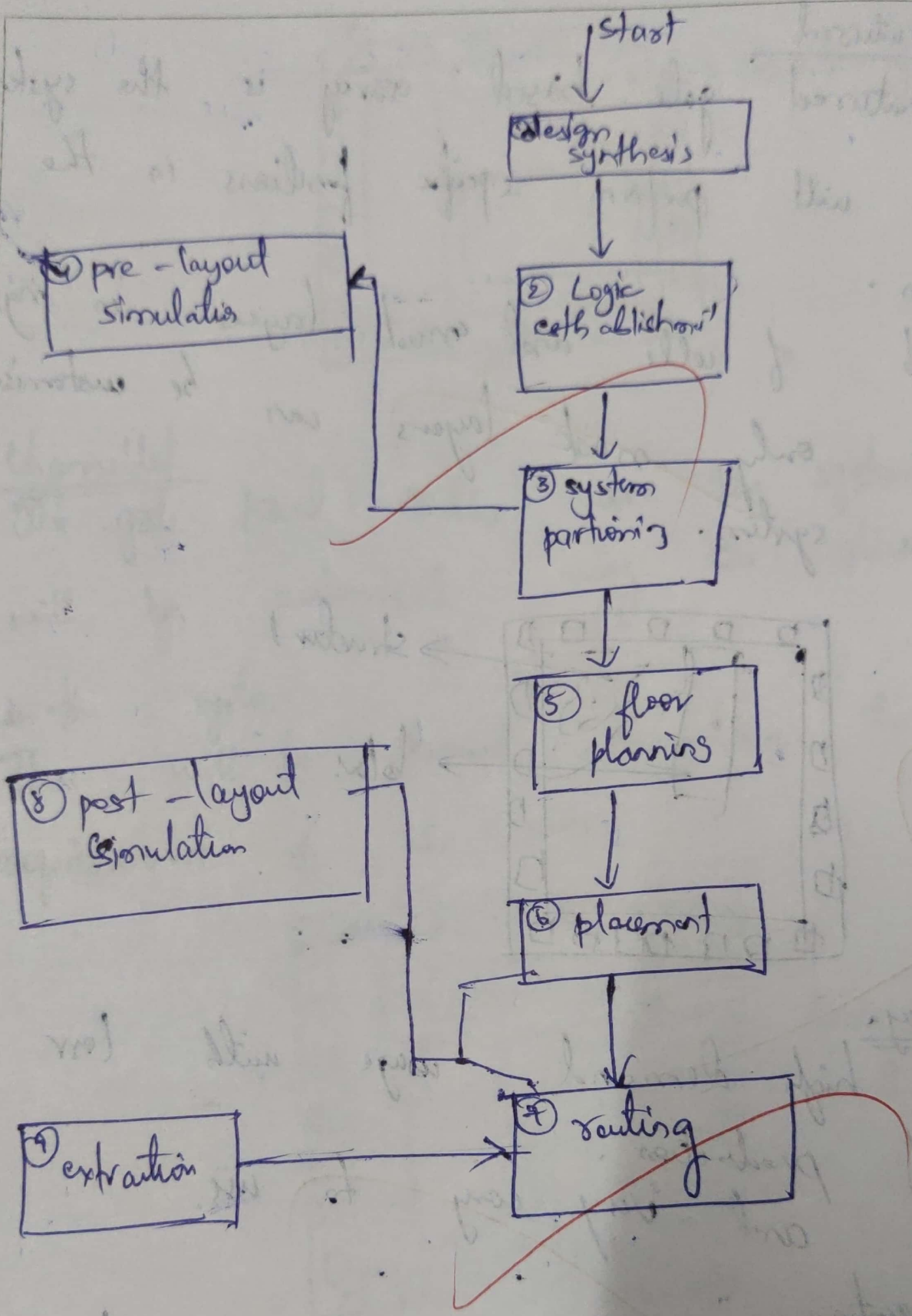
> It is high demand usage with low cost of production.

> Reliable and very easy to use.

Disadvantage

> The manufacturing process can take long time due to its durability and various powers in the chip of the system.

3. Ans



ASIC - design process

> The designing of various steps for better performance of the system is called as ASIC design process.

> It includes the following steps in the process:

① Design Synthesis

> Design synthesis is the process of designing the ASIC in the various logic levels like Verilog and VHDL. However, HDL has become the most important procedure due to the modernized era.

② Logic esth ablishment

> After this the main step to build the logic of the netlist in order to give the correct instructions in the system for the placement.

③ System partitioning

> The designed process is divided into various blocks in the system.

④ Pre-layout Simulation

> This is a necessary step to check whether all the process is working correctly until this part.

⑤ Floor planning

> Floor planning is done to divide the blocks with specific set of instruction.

⑥ Placement

> Placement is done to vary the instruction set with a particular amount of instruction set.

⑦ Routing

> Routing is done to provide the interconnect among various systems in the ASIC design process.

(8) Extraction

> Extraction is done to check the correct resistance and capacitance in the system.

(9) Post - Layout Simulation

> Post - layout simulation is the process of checking whether the designed ASIC is working correctly or not.

The step process from 1 - 4 are called as logical process.

The step process from 5 - 9 are called as physical process.

Together with all these steps form a ASIC design process.

5. Ans

Booths Algorithm

> Multiplication of two signed bits with its complement.

Ex:

Multiplicant (M): 0 0010 11

Multiplier (Q): 0 1110

Multiplier can be converted as

0 1110 0 — — — —

$\Rightarrow 2^{j+1} - 2^i$

Multiplier (Q): 0 1110 $= 2^{3+1} - 2^1$

$= 2^4 - 2^1$

Multiplication of M x Q

$M \times Q = M(2^4 - 2^1)$

$= 2^4(M) - 2^1(M)$

$= 2^4(M) + 2^1(\overline{M})$

$M \times q = 2^{j+1}(M) + 2^{j}(\bar{M})$

$2^{4}(M)$ 01011 × 2^{4}

= 010110000

$2^{1}(\bar{M})$ = 01011

$\bar{M}$ = 10101

$2^{1}(\bar{M})$ = 10101 × 2^{1}

= 101010

In order to make $2^{1}(\bar{M})$ of same the LSB content is to LSB and MSB number will append at MSB.

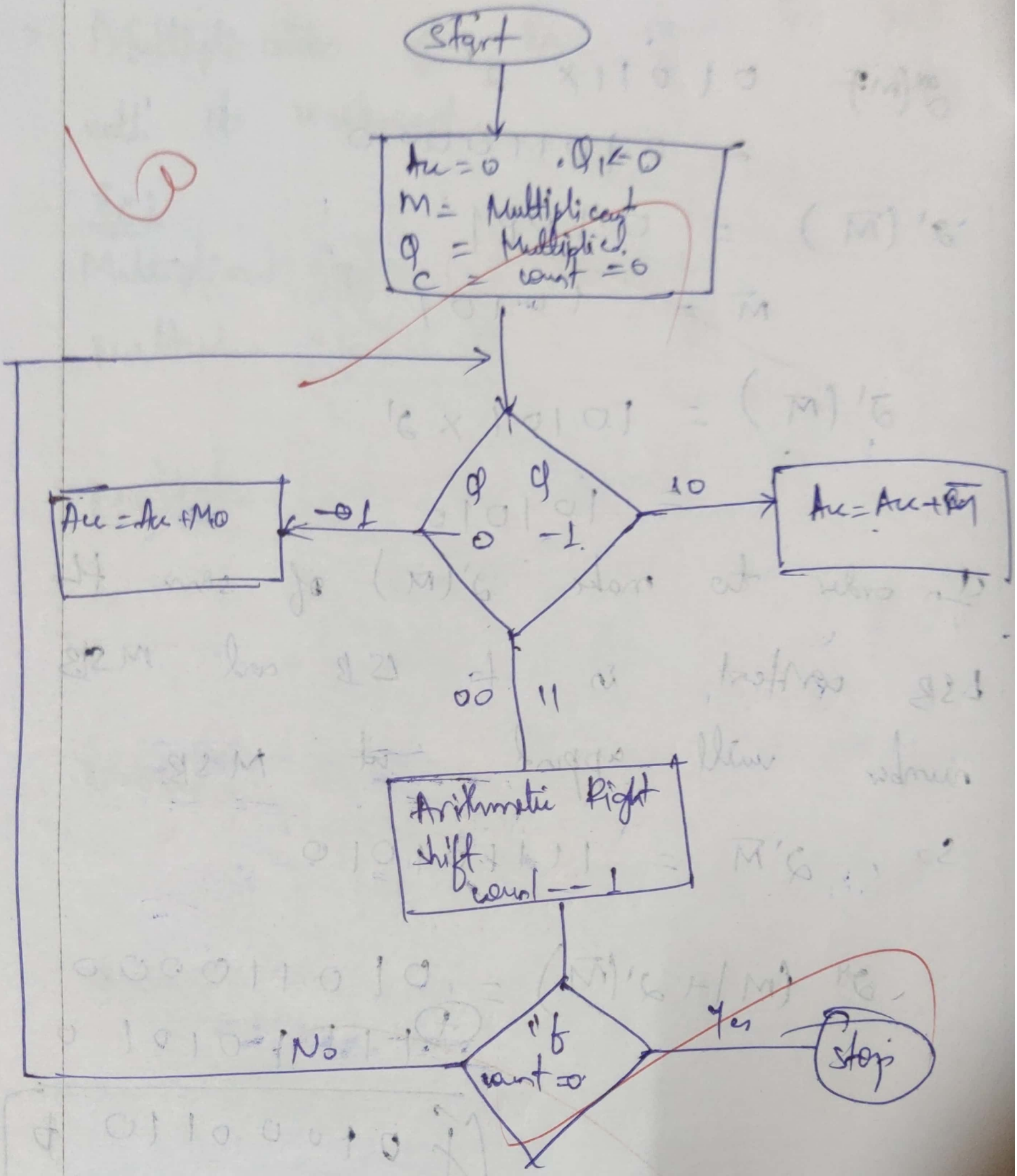
So, $2^{1}\bar{M}$ = 111101010

$2^{4}(M) + 2^{1}(\bar{M})$ = 010110000

(+) 111101010

1 010000110 b

Flow diagram



Implementation of Booth's Algorithm:

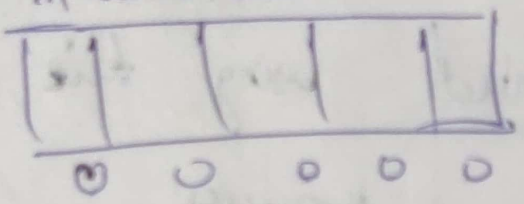
Multiplicand (M) : 0 1011 M = 10101

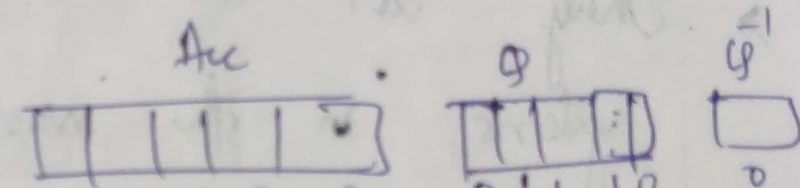
Multiplier (Q) = 01110

Let us take A register as M

Now consider accumulator for operation.

If content MXQ contain same block of zeros Accumulator.





Q_0	Q_{-1}	Operation
0	0	Right shift
0	1	Acc ← Acc + M, AR
1	0	Acc ← Acc + M, AR
1	1	Arithmetic Right Shift

0 0 0 0 0 0 1 1 1 0

⊕ 1 0 1 0 1

1 0 1 0 1 0 0 1 1 0

1 1 0 1 0 1 0 0 1 1 0

1 1 1 0 1 0 1 0 0 1 1 0

⊕ 0 1 0 1 1

1 0 1 0 0 1 1 0 1 0 0 1

0 1 0 0 1 1 0 1 0 0

6. Ans Programmable Logic Devices are those which are done to perform specific functions and desired application process.

(a) Simple Programmable Logic Devices (SPLDs)

> These are the logic devices which are considered in micro-electronic systems.

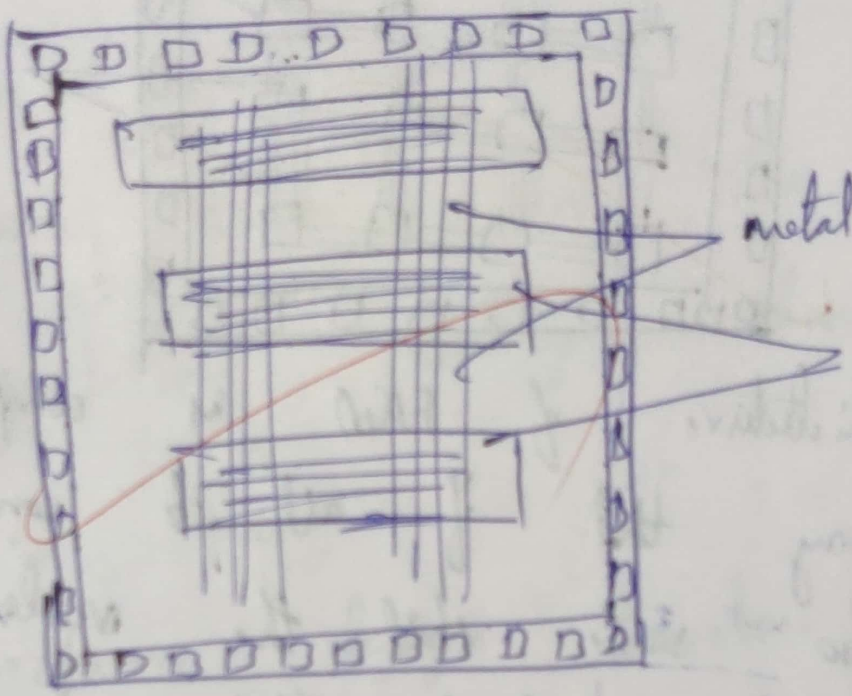
> They can be customized using the systems in the various processes.

> They are logically made to function using the simple system like (AND, OR, multiplexers) etc.;

> Their data can be erased or readable based on the structure they are made up of

> The electronic calls programmable ROM or EPROM can change its characteristics with the high voltage.

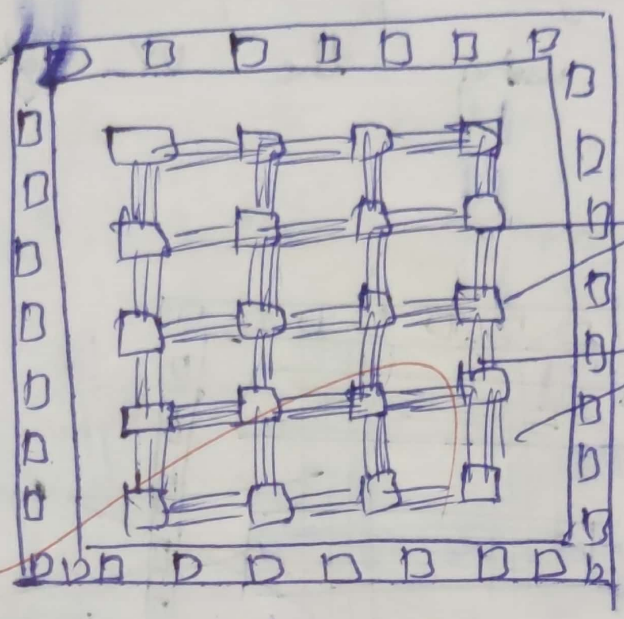
> The mask layers of simple cell can also be altered using the UV light at high voltage.



(B) Field Programmable Gate Arrays

> Field programmable gate arrays are the structures that are complex than basic level programmable devices.

> These consists of various levels of cells with mask layers arranged at each level of the system.



> The architecture of FPGA is complex in such a way that if all its components are also same that the vendors consider it as basic levels PLCs and high level PLCs.

> These FPGA are associated with load based circuitary system to enhance the capability of the system associated with load cycle.

Ans > Verification process involves the processes of testing and verifying the functionalities obtained to design functionalities.

Verification team involves the testing of the bugs and identifying those with the predefined ones.

The hardware design involves the process of meeting specific requirements set by the term for the functionality at different levels.

The system specific functionalities like whether it is working correctly or not whether having any bugs in the system.

> Verification process occurs from the base level of the system, looks over all the working components of the system.

> To fix and identify the bugs the verification team is over-looked in the system for doing its functionality.

> The main intention of the verification team is to obtain the values of output is such a way that it meets the conditions of the pre-defined in the simulation process:

> This will help in obtaining the statutory conditions in the systems.

Testing At Different Levels:

Testing is necessary in any simulation because of the validating it with various levels of the test-cases.

(i) Block Level Testing

> This kind of testing occurs with the testing at various levels of blocks of the system to provide the correct output.

(ii) Integration Level Testing

> This kind of testing is done in the system at various integration levels to perform the basic functionalities of the system.

(iii) System Testing

> System Testing involves testing of the units of the system whether it is functioning correctly or not.

(iv) Schematic Level Testing

> Schematic Level Testing occurs during the simulation to running all the required test cases to give properly the output.

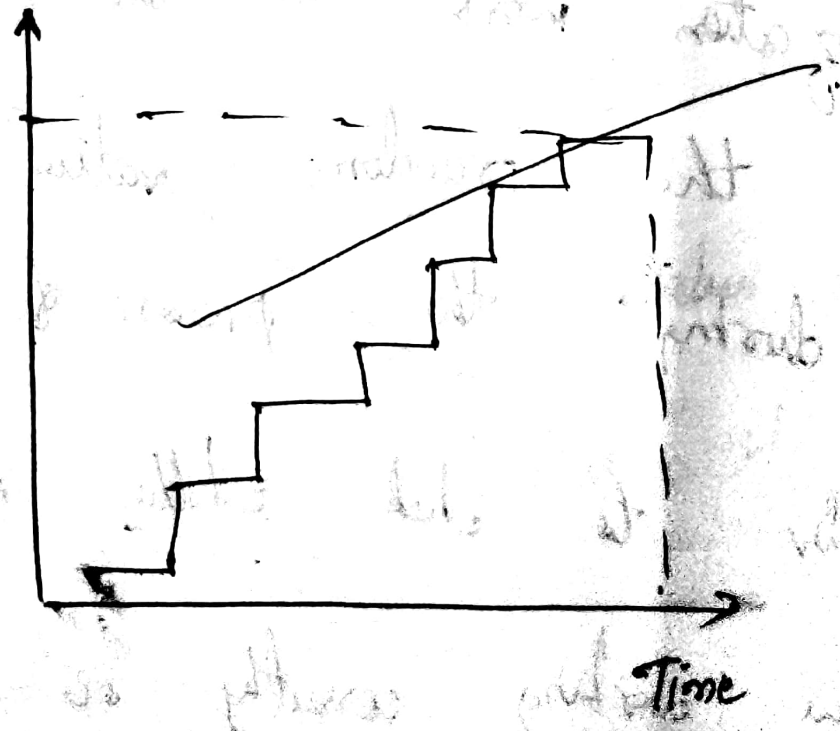
(v) Testing is done over various test-case to identify whether for which test case the is working correctly for the provide input in the system at design level.

(vi) Here, verifying it at various test-bench prop and locating it at different properties gives the hardware design at various levels for the system.

5. Ans (A) Constrainted Random Stimulus

The output obtained to the system must be constrainted at various different levels of the system.

The outputs of the system is to be verified with the coverage time whether it is varying linearly or in a statistical manner for the development of the various kind of outputs.



> The randomly generated values are to be constrained and verified with the input of the system.

> The graph of the randomly generated values to that of the time is in a linear manner which justifies that the given test-cases are working correctly.

(b) Randomization

> Randomization works on the principle of providing the random values to the system during the process of simulation in order to check whether the given inputs are working correctly or not.

7 The assigned value will undergo testing at different levels from basic to the very constrained level to verify both the input and the output value of the system.

(e) Functional Coverage

> Functional coverage occurs when the testing occurs with the functions at different levels of the system while providing the input and outputs of the system with generating the random value in the system and verifying whether it is in correct position or not.

(d) Test Bench Components

> Test Bench components involve combining the test cases at different level to check whether the given verilog code is working for the test-cases or not.

> This can be done at various levels of the system.

(e) Layered Test Bench

> Layered test bench is done at various levels like at each step of the given schema or the code to verify it at each level of the input system to look at various level like monitor test-bench.

6. Ans System Verilog contains various types of built-in data types to work variety of the code by the process of test-bench or randomization it can be verified at different levels of the system.

(a) integer

> Integer is a built-in-data type that contains a whole number to represent the output in the given form. It will always try to store the data.

Ex = n = 'b2222
n = 1234567890

> It will store the value and then represent the data in that form of the output.

> Integer contains various forms like long -int, short -int which comes to use at various levels.

(b) Logical

> Logical comes to the use when there is need to perform a specific operation in the system.

> This will help to provide the usage of various different levels in the system

> Ex: 10000 OR 1111

> OR perform the logical kind of operation in the provided example in the system.

(c) Real Type

> Real type of built-in data type performs the operation like storage at it will store various kind of values in the system.

> The real type will provide various information in the systems without actually justifying the data.

> Ex: ff[3:0] = 1000

> Here [3:0] represents the data is being justified from the zeroth level to the third level of the system.

(d) String Type

> String type helps in storing the characters in the function.

> These determined characters are then verified at various levels for the system.

> Ex: x = "VLSI"

(e) Bitwise Type

> Bitwise type helps in performing the operation at the different wage limits while performing the letter at various levels while performing the system with the verified integrity.

3. Ans # Importance of I/O planning:

The importance of I/O planning requires the various level checking at different levels like given below:

(i) System Integration:

> System integration is checked whether the given input is verifying at different levels or not.

(ii) Scalability

> Scalability is checkdl at various levels at the determining it at various level of the system for ensuring and betterment of the system.

(iii) Complexity :

> Checking complexity is one of the major level manufacturing at the levels to check whether the compatibility is at good level or not.

Importance of Power planning :

(i) Thermal distribution :

> The power to be distributed to the system must be checked at the levels for identifying at the different level of the system; whether any extra power consumption is happening or what. It is to increase the efficiency of the system.

(ii) Increased Efficiency

> It is to increase the efficiency at the various different levels of the system whether proper current distribution is happening or not.

(iii) Compatibility

> This is very important step in the floor planning as it is done at each level of the system to check whether it is meeting the specifications set by the functionality or providing and dependent on the system at various levels.

Placement of I/o pads & power distribution

Work:

> The placement of the I/o pads must be done between the cells so that their compatibility is best at the different levels of the system.

> Power distribution must be done in an equal manner between all the I/o pads present to ensure they are working in a correct manner to meet the system requirement of the given I/o pads.

> Here, in this manner the I/o pads and power distribution is done to check and meet all conditions in system.

1. Ans > The primary goals and objectives of floor planning are

(i) Designing
(ii) Placement
(iii) Modification

(i) Designing :

> Designing of the floor planning must be in such a way that all the wires and the coils must be placed in the parallel way to determine the equality among the system provided during the specification.

> If any mistake lead in the designing process then there won't be the proper placement of the wires and the coils.

(ii) Placement

> Placement of the I/o pads must be done to between and the cells so that their compatibility is best at different level of the system.

> After the placement of the rings and the cells the power distribution comes to the major role in the system at various verified levels of the system.

(iii) Modification

> Later, if there is is any mistake to the placement of I/o pads then the modification is done at various levels of the system.

Methods to measure delay in floor planning

(i) RC Delay :

> RC delay is the major kind of delay that occurs in the system, this is affected during the variation of the capacitance performance to the system.

(ii) Schematic Test Delay :

> Schematic Test Delay will occur if the output does not matches with the objectives set by the design specification at various level of the system.

> Schematic Test Delay is checked at the various level like representing from basic to high level.

Wire Length

> Wire length plays a major role in determining the signal delay of the system.

> The wires and the coils "get in" the narrow steps while determining for the system requirements of the floor planning.

Capacitance

> Capacitance comes into effect with the RC delay at various major roles, once if the capacitance is varied then it will have to look at different levels of the system to check the compatibility.