CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Design a combinational logic truth table so that an output is generated indicating when a majority of four inputs is tree.	4	L3	CO1
	b.	Find the prime implicants and the essential prime implicants of the following Boolean functions using Karnaugh maps. i) $f(a, b, c, d) = \Sigma(1, 5, 6, 7, 11, 12, 13, 15)$ ii) $f(a, b, c, d) = \Sigma(0, 1, 4, 5, 9, 11, 13, 15)$	8	L4	CO1
	c.	Simplify the given boolean function using Quine McCluskey minimization technique for the function $O = f(a, b, c, d) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$	8	L3	CO1
		OR			
Q.2	a.	Place the following equations into the proper canonical form: i) $P = f(a, b, c) = ab' + ac' + bc$ ii) $G = f(w, x, y, z) = w'x + yz'$	4	L3	CO1
	b.	Find the minimal sum and minimal product for the following Boolean functions using Karnaugh maps i) $f(a,b,c,d) = \bar{a}\bar{b}d + bcd + a\bar{b}d + b\bar{c}\bar{d}$ ii) $f(a,b,c,d) = (a+\bar{b})(a+c+d)(\bar{a}+\bar{b}+\bar{d})(a+\bar{c}+d)$	8	L4	CO1
	c.	Simplify the given boolean function using quine. McCluskey minimization technique for the function. $s = f(a,b,c,d) = \Sigma(1,3,13,15) + \Sigma d(8,9,10,11)$	8	L3	CO1
		Module – 2			
Q.3	a.	Design and explain binary full adder with block diagram, Karnaugh map and logic circuit.	10	L3	CO2
	b.	Define decoder, write the symbol, truth table and logic circuit for 3:8 line decoder using minterm generator.	10	L2	CO2
		OR			
Q.4	a.	Define multiplexer, write the symbol, truthtable and logic circuit for 4:1 multiplexer using enable input.	10	L2	CO2
	b.	Realize the Boolean function $f(w, x, y, z) = \Sigma(0, 1, 5, 6, 7, 9, 12, 15)$ i) Using 8:1 MUX ii) Using 4:1 MUX	10	L2	CO2

		Module – 3			
Q.5	**a.**	Develop the characteristic equation for i) SR flip flop ii) JK flip flop iii) D flip flop iv) T flip flop.	**10**	**L3**	**CO3**
	b.	Explain serial in, parallel at unidirectional shift register and parallel in serious out unidirectional shift register.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Explain Mod-4 ring counter and Mod-8 twisted ring counter with logic diagram and counting sequence.	**10**	**L2**	**CO3**
	b.	Design a synchronous Mod-6 counter using clocked D-flip flop.	**10**	**L3**	**CO3**
		Module – 4			
Q.7	**a.**	Explain logical operators and relational operators used in verilog.	**8**	**L2**	**CO4**
	b.	Illustrate i) NETS ii) Register iii) Vector iv) integer data types with an example.	**8**	**L2**	**CO4**
	c.	Write a verilog code for full adder using data flow description style.	**4**	**L2**	**CO4**
		OR			
Q.8	**a.**	Illustrate the structure of behavioural description with an example using half adder.	**8**	**L2**	**CO4**
	b.	Illustrate the structure of verilog module with an example using half subtractor.	**8**	**L2**	**CO4**
	c.	Write a verilog code for binary to gray using behavioural description style.	**4**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Write the syntax of IF and EISE-IF with an example.	**8**	**L2**	**CO4**
	b.	Write logic symbol, flowchart and program for D-latch using behavioural description style.	**8**	**L2**	**CO4**
	c.	Write a verilog code for 8:1 MUX using behavioural description style.	**4**	**L2**	**CO4**
		OR			
Q.10	**a.**	Explain the structure of structural model with built in gates using example of half adder. Also mention an primitive built in gates.	**8**	**L2**	**CO4**
	b.	Write a verilog code of a 3-bit ripple carry adder using structural description model.	**8**	**L2**	**CO4**
	c.	Write a verilog code of SR flip flop using behavioural description style.	**4**	**L2**	**CO4**

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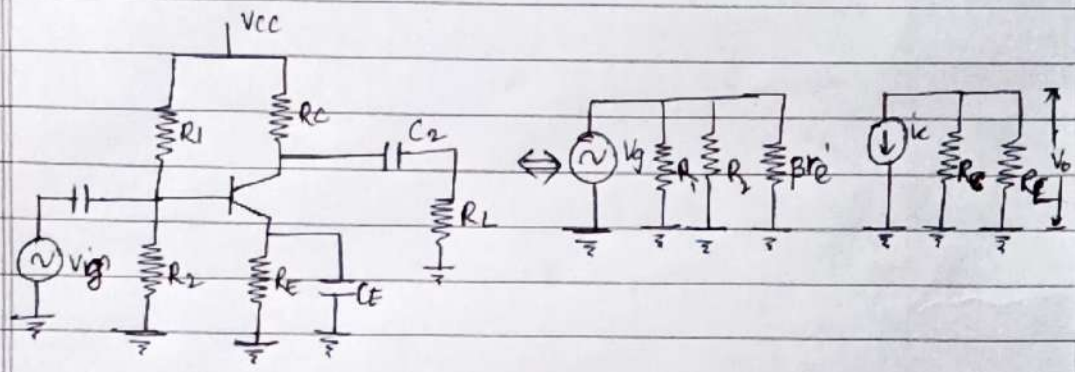
Electronic Principles and Circuits

Module - I

1(a) Derive expressions Vin, Vout and A_V for a common emitter circuit with ac equivalent circuit with Π-model.

→



▲ Common Emitter circuit & its AC equivalent circuit using Π-model.

- Using Ohm's law, the I/P voltage can be expressed as:

$$\boxed{V_{in} = i_b \beta r_e'}$$

- In the collector circuit, the ac O/P voltage:

$$V_{out} = i_c (R_c \| R_L)$$

$$\Rightarrow V_{out} = \beta i_b (R_c \| R_L) \quad \left[\because \beta_{ac} = \frac{i_c}{i_b}\right]$$

- Voltage gain is given by $A_V = \frac{V_{out}}{V_{in}} = \frac{\beta i_b (R_c \| R_L)}{i_b \beta r_e'}$

$$\boxed{A_V = \frac{R_c \| R_L}{r_e'}}$$

- Expression for ac collector resistance $r_c = R_c \| R_L$

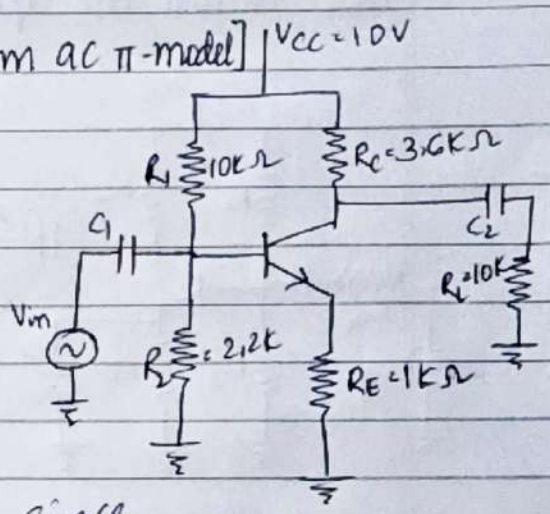
$$\therefore \boxed{A_V = \frac{r_c}{r_e'}} \quad \text{where } r_e' = \frac{25mV}{I_{EQ}}$$

1(b) What is the voltage gain and output voltage across the load resistor of V_{DB} amplifier?

→ Given: $R_1 = 10K\Omega$, $R_2 = 2.2K\Omega$, $R_C = 3.6K\Omega$, $R_E = 1K\Omega$, $R_L = 10K\Omega$, $V_{CC} = 10V$, $V_{BE} = 0.7V$, $V_{in} = 2mV$.

W.K.T: $A_V = \frac{R_C \| R_L}{r_e'}$ [from ac π-model]

& $r_e' = \frac{25mV}{I_{EQ}}$



• From the circuit,

$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$

$= \frac{10 \times 2.2K}{10K + 2.2K}$

$= 1.80V.$

$V_{BE} = V_B - V_E.$

$V_E = V_B - V_{BE}$

$= 1.80 - 0.7$

$\boxed{V_E = 1.1V}$

Since,

$V_E = I_E R_E$

$I_{EQ} = \frac{V_E}{R_E}$

$= \frac{1.1}{1K} = 1.1mA.$

$\therefore r_e' = \frac{25mV}{1.1mA} = 22.727\Omega$

$\therefore A_V = \frac{R_C \| R_L}{r_e'} = \frac{3.6K \| 10K}{22.73} = \frac{2.64K}{22.73}$

$\boxed{A_V = 116.14}$

• W.K.T: $A_V = \frac{V_{out}}{V_{in}}$

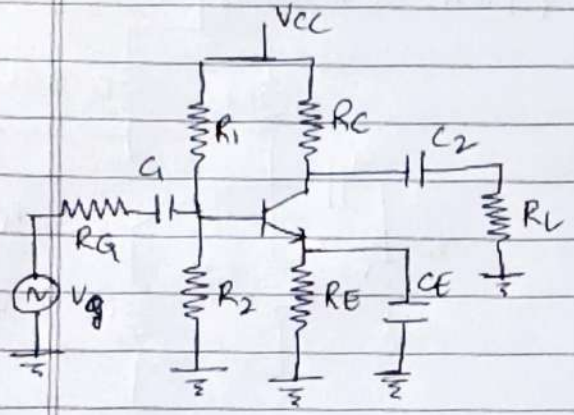
$\therefore V_{out} = A_V \cdot V_{in}$

$= 116.14 \times 2mV$

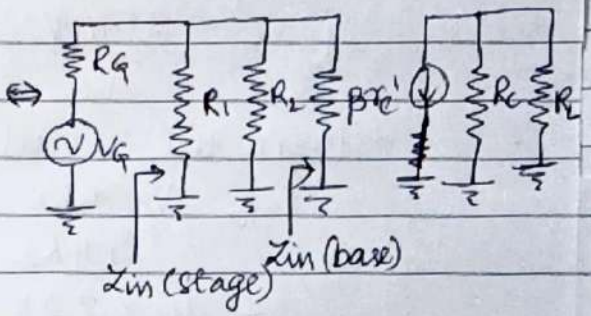
$\boxed{V_{out} = 0.232V}$

2 (a) With a neat diagram explain loading effect of input impedance.

→ • To analyze the loading effect of I/P impedance, we use a source resistor or generator resistor (R_G) across the I/P voltage supply.



▲ CE amplifier.

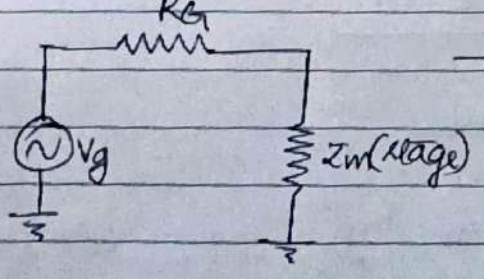


▲ ac equivalent π-model

• Due to some voltage drop across R_G, the net AC -voltage across the emitter diode will decrease.

• The I/P impedance includes the effects of the biasing resistors R_1 & R_2, in parallel with the input impedance of base $Z_{in(base)}$.

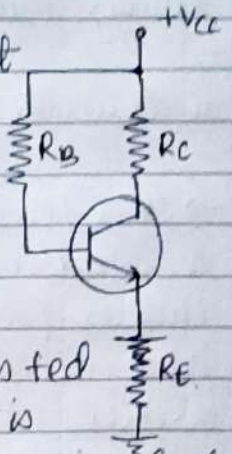
• Input impedance at stage: $Z_{in(stage)} = R_1 \| R_2 \| \beta r_e'$
• Input impedance at base: $Z_{in(base)} = \beta r_e'$



→ With voltage divider theorem, we can write:

$$V_{in} = \frac{Z_{in(stage)} \times V_g}{R_G + Z_{in(stage)}}$$

2(b) (i) Emitter-Feedback Bias:



- Basic idea of this Bias circuit is:

→ If I_C increases, V_E increases causing fall in V_B which leds to less I_B which is opposing original increase in I_C.

→ In this bias Emitter voltage is fed back to the base circuit & it is negative because it opposes the original change in I_C stabilizing Q-point.

→ But this bias circuit is not much popular, because Q-point variation is still too large.

→ Equations of Emitter feedback bias:

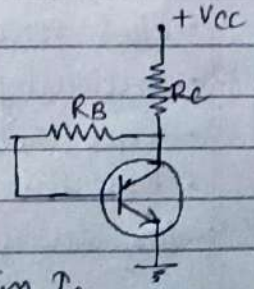
$$I_E = \frac{V_{cc} - V_{BE}}{R_E + R_B/\beta dc}$$

$$V_E = I_E R_E$$

$$V_B = V_E + 0.7V$$

$$V_c = V_{cc} - I_c R_c.$$

(ii) Collector Feedback bias:



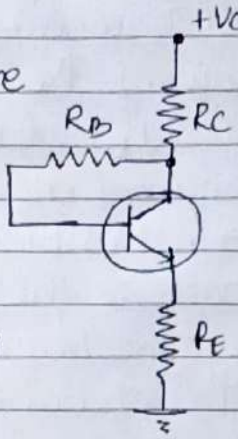
- Also known as self-bias.
- Suppose, if I_C increases, it decreases V_C → decreases V_B inturn decreasing I_B, which again opposes original increase in I_C

→ Hence, it uses a negative feedback in attempt to reduce original change in collector current.

$$I_E = \frac{V_{cc} - V_{BE}}{R_c + R_B/\beta dc}, \quad V_B = 0.7V, \quad V_c = V_{cc} - I_c R_c$$

• Collector-feedback bias is more effective than emitter-feedback in stabilizing Q-point

(iii) Collector & Emitter Feedback bias:



→ This feedback bias is more a combination of both Emitter feedback bias ckt and collector feedback bias circuit.

• Analyzing equations are:

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_E + R_B/\beta_{dc}}$$

$$V_E = I_E R_E$$

$$V_B = V_E + 0.7V$$

$$V_C = V_{CC} - I_C R_C.$$

3(a) The three biasing modes to bias MOS amplifier are:

(i) Biasing by fixing V_{GS}:

• Most straightforward method to bias a MOSFET.
• Initially V_{GS} is varies to get required I_D.
• Once adequate I_D is obtained, V_{GS} is fixed.
• But, this biasing is not a good approach due to following reasons

W.K.T: $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

• Values of μ_n, C_{ox}, $\frac{W}{L}$, V_t vary for two different MOSFET's. Both μ_n & V_t depend on temperature

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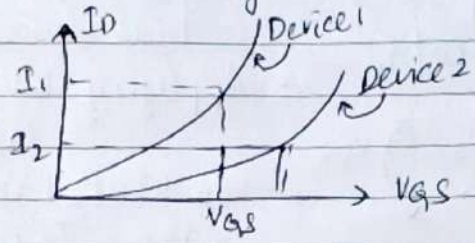
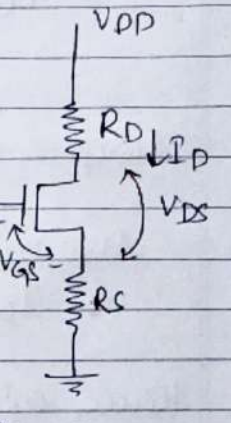
• Hence, if we fix V_{GS}, I_D becomes very much temperature dependant, due to which variability of I_D increases very much.



(ii) Biasing by fixing V_G and connecting a resistance in the source.



We can write, By KVL,

$$V_G = V_{GS} + R_S I_D \quad \text{—①}$$

$[\because I_D = I_S]$

& $V_{GS} = V_G - V_S$

$V_D = V_D - V_S$.

• In eqⁿ ①, if V_G is much greater than V_{GS}, I_D will be mostly determined by values of V_G & R_S.

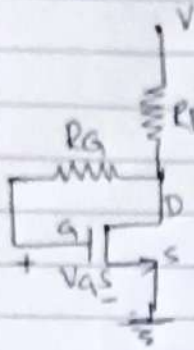
• However, if V_G is not much greater than V_{GS}, resistor R_S provides negative feedback which acts to stabilize the values of bias current I_D.

• Eqⁿ ① indicates that since V_G is fixed, V_{GS} will have to decrease, but this inturn decreases I_D

• Thus the negative feedback action of R_S keeps I_D as constant as possible.

• It reduces the variability I_D, hence stabilizing Q-point.

(iii) Drain to gate Feedback Resistor:



- Negative feedback increases bias stability.
- Applying KVL to drain to source loop:

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DD} = I_D R_D + V_{DS} \quad \text{—①}$$

From circuit, $V_G = V_D$

$$V_{GS} = V_G - V_S = V_D - V_S = V_{DS}$$

$$\therefore \boxed{V_{GS} = V_{DS}}$$

Therefore, eq^n ① can also be written as:

$$V_{DD} = I_D R_D + V_{GS} \quad \text{—②}$$

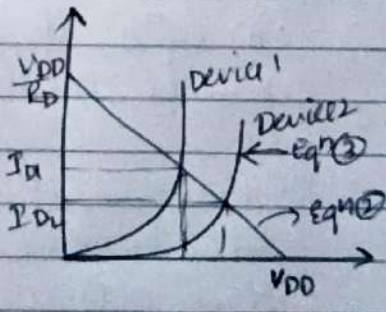
Also in saturation,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \quad \text{—③}$$

Hence, eq^n ② can be written as

$$I_D = \left(\frac{-1}{R_D}\right) V_{GS} + \frac{V_{DD}}{R_D}$$

$$y = mx + c$$

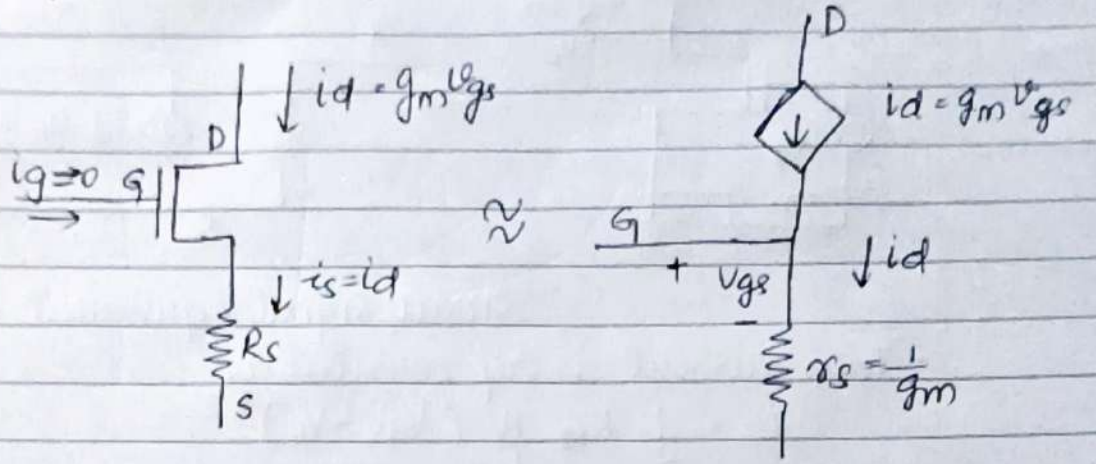


→ If temperature increases, I_D should reduce, which inturn reduces V_{GS}

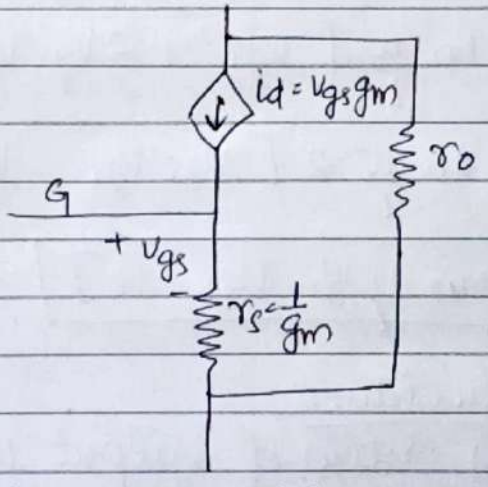
- According to drain characteristics, if V_{DS} ↓se, I_D ↓se, which opposes initial assumption.
- Hence, here the negative feedback resistor R_G comes into action. It maintains I_D current a constant as much as possible.
- Hence, Q-point will be stable.

3(b) Explain the T-equivalent circuit model of MOSFET.

→

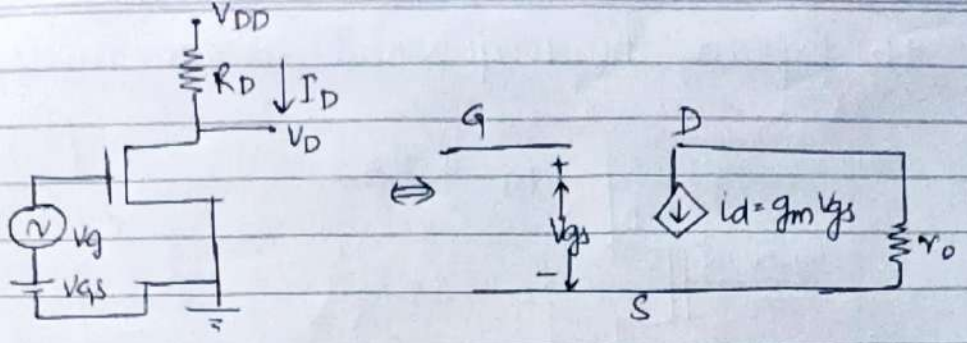


- Figure shows T-equivalent model of MOSFET without internal resistance r_o.
- By including the internal resistance r_o, the t-equivalent model can be redrawn as



- T-equivalent model is preferred when source resistance r_s is included.
- Π-model is preferred if source resistance r_s is absent.

4(a) With a small-signal equivalent model of MOSFET, derive an expression of voltage gain and transconductance.



Small signal equivalent model.

- Total current is represented as:

$$i_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} K_n \frac{W}{L} [V_{GS} + V_{gs} + (-V_t)]^2$$

→ Total ac component can be obtained by considering only ac components

$$i_d = \frac{1}{2} K_n \frac{W}{L} [\cancel{V_{gs}^2}^{0} + 2 V_{gs} V_{GS} - V_{gs} V_t]$$

$$i_d = \frac{1}{2} K_n \frac{W}{L} 2 [V_{GS} V_{gs} - V_{gs} V_t]$$

$$\boxed{i_d = K_n \frac{W}{L} V_{gs} [V_{GS} - V_t]}$$

Trans conductance:

- Defined as ratio of output to the I/P voltage

$$g_m = \frac{\text{O/P current}}{\text{I/P voltage}} = \frac{i_d}{V_{gs}}$$

we have: $i_d = K_n \frac{W}{L} [V_{gs} (V_{GS} - V_t)]$

$$\frac{i_d}{V_{gs}} = K_n \frac{W}{L} \left[\frac{V_{gs}}{V_{gs}} (V_{GS} - V_t)\right]$$

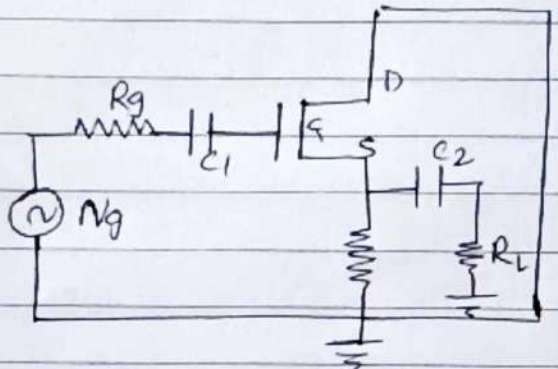
$$\boxed{g_m = \frac{K_n W}{L} (V_{GS} - V_t)}$$

• Voltage gain $A_V = \frac{V_{out}}{V_{in}} = \frac{V_{ds}}{V_{gs}} = \frac{i_d R_D}{V_{gs}}$

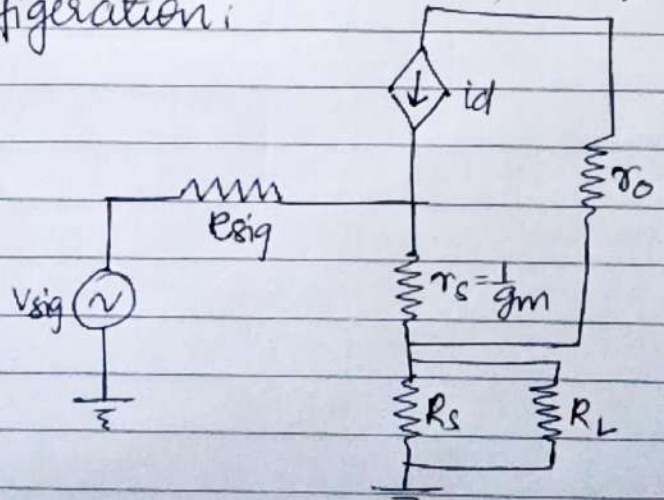
$$A_V = g_m R_D$$

4(b) Explain common source follower and derive the expression of voltage gain with necessary equation.

→ The common-Drain configeration of MOSFET is known as common soure follower.



Step1: ac equivalent T-model of common Drain configeration:



Step2: Input & Output Resistance.

$R_{in} = \infty$ (due to Gate insulation)

$R_{out} = r_o \,||\, \frac{1}{g_m}$

Step3: $A_V = \frac{V_{out}}{V_{in}} = \frac{R_S}{R_S + \frac{1}{g_m}}$

$$V_{out} = \frac{V_{in} R_S}{R_S + \frac{1}{g_m}}$$

$$\Rightarrow \boxed{A_V = \frac{g_m R_S}{1 + g_m R_S}}$$

R/2R ladder D/A converter

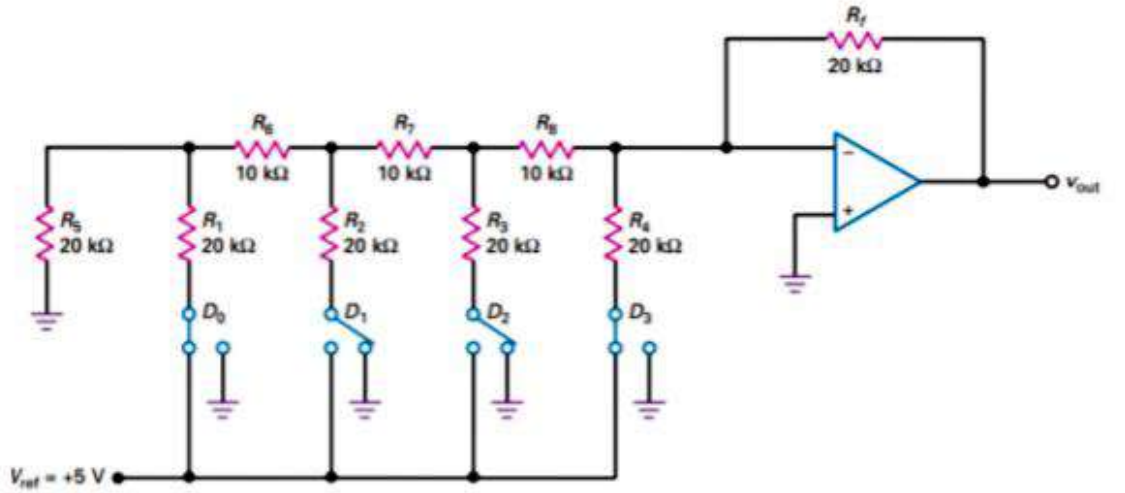


Fig 18-25

A 4-input D/A converter has 16 possible outputs, an 8-input A/D converter has 256 possible outputs, and a 16-input D/A converter has 65,536 possible outputs. This means that the negative-going staircase voltage of Fig. 18-24b can have 256 steps with an 8-input converter and 65,536 steps with a 16-input converter. A negative-going staircase voltage like this is used in a digital multimeter along with other circuits to measure the voltage numerically. The binary-weighted D/A converter can be used in applications where the number of inputs is limited and where high precision is not required. When a higher number of inputs is used, a higher number of different resistor values is required. The accuracy and stability of the D/A converter depends on the absolute accuracy of the resistors and their ability to track each other with temperature variations. Because the input resistors all have different values, identical tracking characteristics are difficult to obtain. Loading problems can also exist with this type of D/A converter because each input has a different input impedance value. The R/2R ladder D/A converter, shown in Fig. 18-25, overcomes the limitations of the binary-weighted D/A converter and is the method most often used in integrated-circuit D/A converters. Because only two resistor values are required, this method lends itself to ICs with 8-bit or higher binary inputs and provides a higher degree of accuracy. For simplicity, Fig. 18-25 is shown as a 4-bit D/A converter. The switches D0 – D3 would normally be some type of active switch. The switches connect the four inputs to either ground (logic 0) or 1Vref (logic 1). The ladder network converts the possible binary input values from 0000 through 1111 to one of 16 unique output voltage levels. In the D/A converter shown in Fig. 18-25, D0 is considered to be the least significant input bit (LSB), while D3 is the most significant bit (MSB). To determine the D/A converter's output voltage, you must first change the binary input value to its decimal-equivalent value BIN.

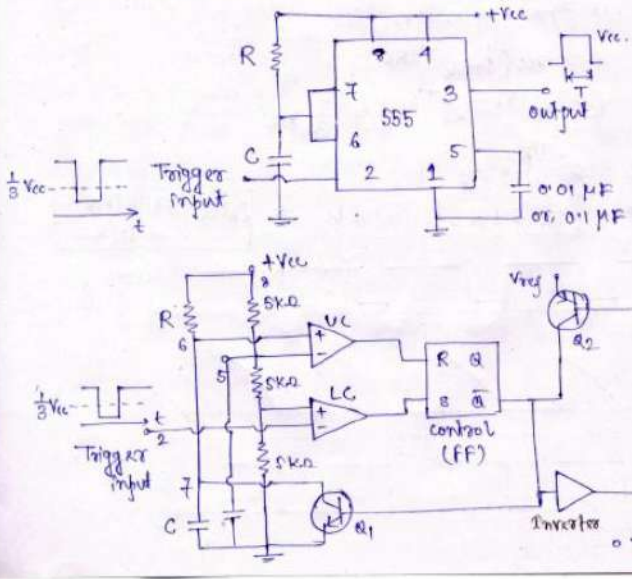
$$\mathbf{BIN} = (D_0 \times 2^0) + (D_1 \times 2^1) + (D_2 \times 2^2) + (D_3 \times 2^3)$$

Then, the output voltage will be found by:

$$V_{out} = -\left(\frac{\mathbf{BIN}}{2^N} \times 2V_{ref}\right)$$

where N equals the number of inputs.

Monostable Multivibrator



Operation

In standby mode, FF holds transistor Q_1 on, thus clamping the external timing capacitor C to ground. The FF is in reset condition. $\therefore \bar{Q} = 1$, o/p = LOW.

As the trigger passes through $\frac{Vcc}{3}$, the FF is set i.e $\bar{Q} = 0$. This makes Q_1 'off' and the short circuit across the timing capacitor is released. As $\bar{Q}$ is LOW, output goes HIGH (=Vcc). The timing cycle now begins. since C is unclamped, voltage across it raises exponentially through R towards Vcc with a time constant RC.

If the voltage across the capacitor is just greater than $\frac{2}{3}$ Vcc and the upper comparator resets the FF i.e R=1, S=0. This makes $\bar{Q} = 1$, transistor Q_1 goes on (i.e saturates), the output returns to standby state (i.e LOW).

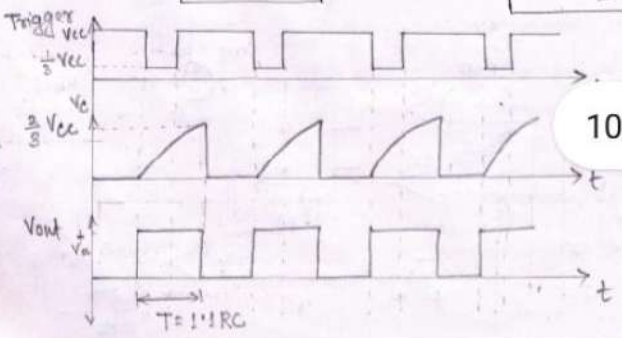
Voltage across the capacitor,

$$V_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

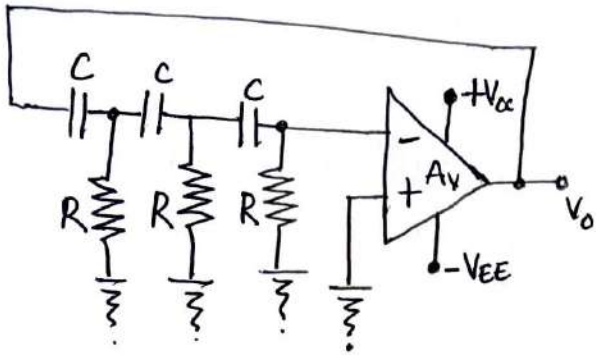
at $t = T$, $V_c = V_{cc}\left(1 - e^{-T/RC}\right) = \frac{2}{3} V_{cc}$

or, $e^{-T/RC} = \frac{1}{3}$

or, $\boxed{T = 1.1RC}$ seconds or, $\boxed{\text{Pulse width (PW)} = 1.1RC}$

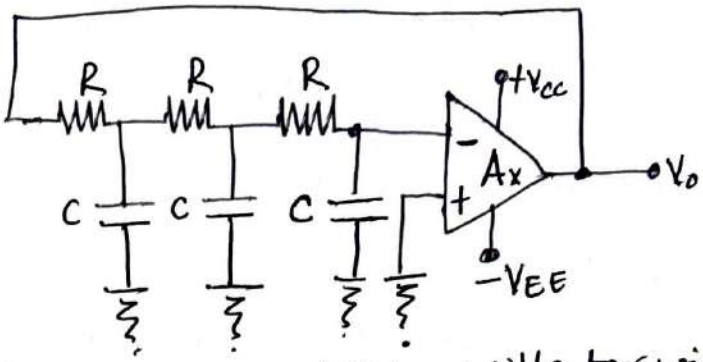


Phase shift Oscillator:



(a) Phase shift oscillator with 3 lead Circuit

$$f_r = \frac{1}{2\pi\sqrt{2N}RC}$$



(b) Phase shift oscillator with 3 lag circuit

$$f_r = \frac{1}{2\pi\sqrt{6}RC}$$

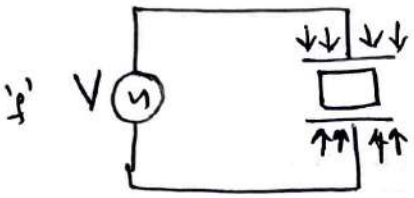
$$B > \frac{1}{29} \quad \therefore A_V > 29$$

- Fig. (a) shows phase shift oscillator with three lead Circuit in feedback path.
- lead circuit produce a phase shift of 0° to 90°
- each lead circuit produce a phase shift of 60°, at some frq.
- The total phase shift of three lead Circuit is 180°
- The amplifier has a phase shift of 180°
- As a result the overall phase shift is 360° (or) 0°
- When $A_VB > 1$, then the oscillations start
- Fig (b) shows the phase shift oscillator with three lag Circuit

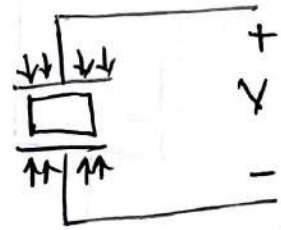
- The operation is similar to fig (a)
- Lag Circuit produces −180° phase shift at some frq
- The amplifier produces a phase shift of 180°
- As a result overall phase shift is 0°.
- If $A_VB > 1$, then the oscillations start.
- This oscillator is not popular circuit
- Problem is that it can not easily adjust to large frq range

Crystal Oscillator:

- These oscillators are used in Radio & Tele communications
- They are used in many digital Circuits
- They are essential part of Micro controllers to generate the clock signals.
- It can generate stable frequencies from 100 KHz to 100 MHz.
- It works on the principle of Inverse-Piezo electric effect.



Inverse piezoelectric effect.

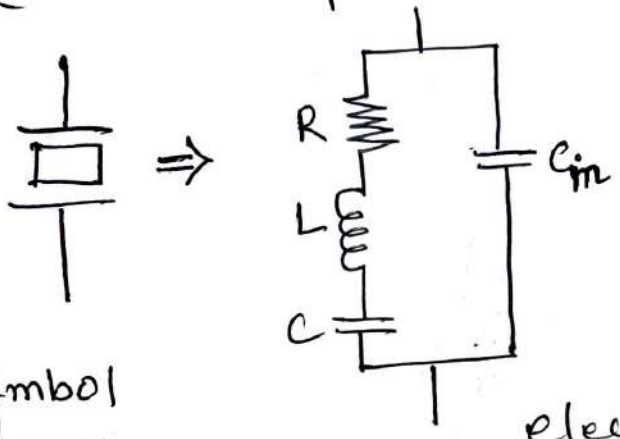


Piezo electric effect.

- when the Piezo electric material is mechanically Vibrated, then they generate the Voltage across the two terminals. This is known as Piezo electric effect.
- Inverse piezo electric effect is reverse operation of Piezo electric effect.
- If certain amount of voltage is applied to Piezo electric material, It will Vibrate and produce some frequency 'f'.
- This natural resonating freq of the Crystal depends on the thickness of the Crystal.

- Hence $f \propto \frac{1}{\text{Thickness of Crystal.}}$

- Commonly used Crystal is Quartz Crystal to produce Sinusoidal oscillations, because
  (i) It is mechanically strong
  (ii) good piezo electric sensitivity
  (iii) less expensive



Symbol

electrical equivalent circuit.

- The above figure shows the Symbol of the Crystal and its electrical equivalent circuit.

- here R → electrical equivalent Resistance of Crystal (Interal Frictions)
  L → electrical equivalent Inductance of Crystal mass
  C → electrical equivalent. Crystal Capacitance
  C_m → Capacitance due to mechanical mounting of Crystal.

- Crystal have two resonent frequencies.
  (i) Series resonent frq
  (ii) parallel resonent frq

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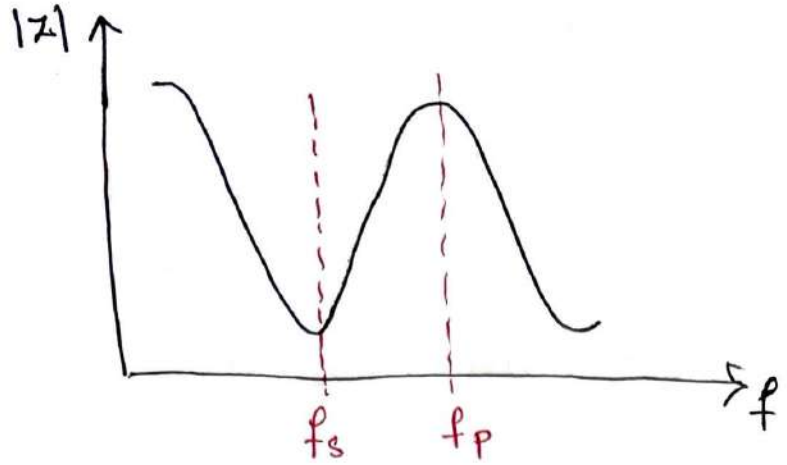
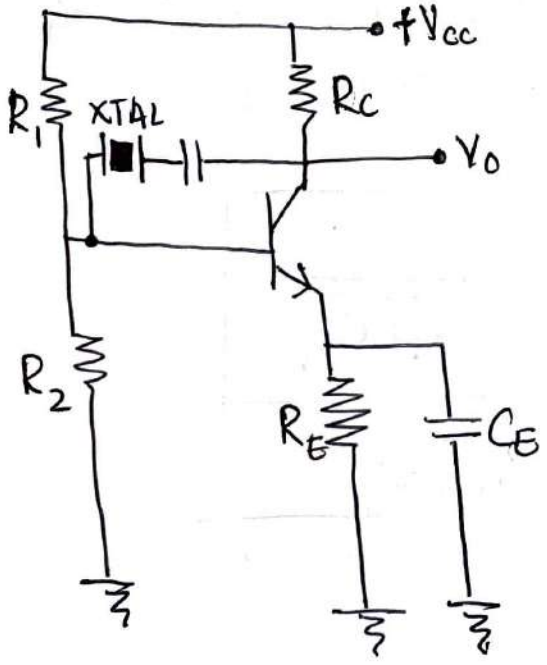
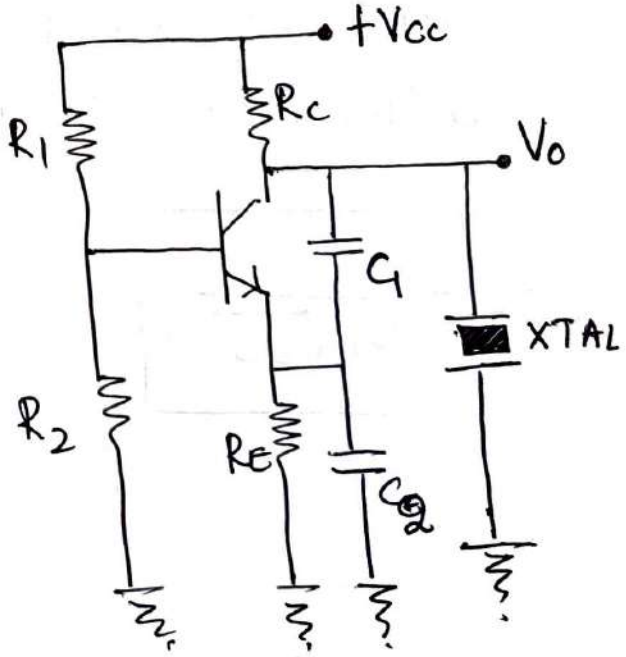


|Z| V/s frq graph

- The figure shows impedence v/s frq graph.
- f_s → Series resonent frq
  f_p → Parallel resonent frq
- When the Crystal is used at series resonent frq, the impedence is low
- When the Crystal is used at parallel resonent frq the impedence is high.



Series Resonant



Parallel resonent

- In both Series & parallel Resonent Circuit, Common emitter Voltage divider is used as an amplifier
- In Series Resonent, the Crystal is Connected as a series element in the feedback
- And in parallel Resonent, the Crystal is connected in parallel.
- Both the Circuit will operate on the principle of Inverse Piezoelectric effect.
- When Voltage is applied the crystal will Vibrate and produce some frequency.
- In the Series Resonent, the impedence is low & the amount of feedback to the Amplifier is high.
- In the parallel Resonent, the Crystal is acting as an inductor, hence the Circuit will work as a Colpitts Oscillator

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$C_{eq} = \frac{C \cdot C_m}{C + C_m}$$

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6c)

Calculate Series Resonant Frequency (f_s)

$$f_s = \frac{1}{2\pi\sqrt{L \cdot C_s}}$$

Substitute the given values:

$$f_s = \frac{1}{2\pi\sqrt{(3)(0.05 \times 10^{-12})}}$$

$$f_s = \frac{1}{2\pi\sqrt{1.5 \times 10^{-13}}}$$

$$f_s = \frac{1}{2\pi(1.2247 \times 10^{-7})}$$

$$f_s = \frac{1}{7.698 \times 10^{-7}}$$

$$f_s \approx 1.298\,\text{MHz}$$

Calculate C'_m (Effective Capacitance)

$$C'_m = \frac{C_s \cdot C_m}{C_s + C_m}$$

Substitute the given values:

$$C'_m = \frac{(0.05 \times 10^{-12}) \cdot (10 \times 10^{-12})}{0.05 \times 10^{-12} + 10 \times 10^{-12}}$$

$$C'_m = \frac{0.5 \times 10^{-24}}{10.05 \times 10^{-12}}$$

$$C'_m \approx 0.04975\,\text{pF} = 0.04975 \times 10^{-12}\,\text{F}$$

Calculate Parallel Resonant Frequency (f_p)

$$f_p = \frac{1}{2\pi\sqrt{L \cdot C'_m}}$$

Substitute the values:

$$f_p = \frac{1}{2\pi\sqrt{(3)(0.04975 \times 10^{-12})}}$$

$$f_p = \frac{1}{2\pi\sqrt{1.4925 \times 10^{-13}}}$$

$$f_p = \frac{1}{2\pi(1.2217 \times 10^{-7})}$$

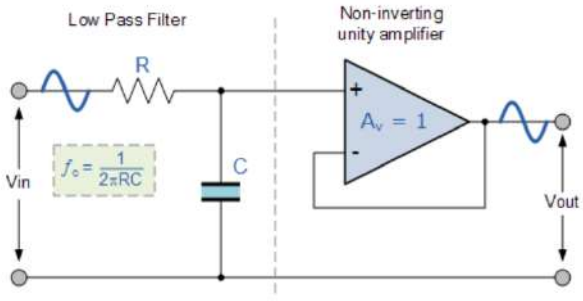
$$f_p = \frac{1}{7.673 \times 10^{-7}}$$

$$f_p \approx 1.303\,\text{MHz}$$

First-Order Low-Pass Filter

A **first-order low-pass filter** is a basic electrical circuit that allows low-frequency signals to pass through while attenuating high-frequency signals. It is called "first-order" because its output depends linearly on the input frequency (i.e., the roll-off rate is 20 dB/ decade).

First Order Low Pass Filter

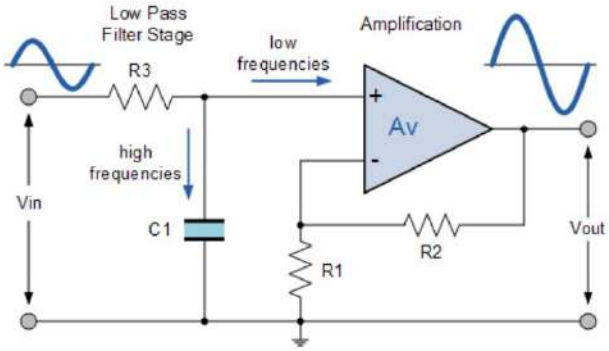


This first-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer) giving it a DC gain of one, Av = +1 or unity gain as opposed to the previous passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

While this configuration provides good stability to the filter, its main disadvantage is that it has no voltage gain above one. However, although the voltage gain is unity the power gain is very high as its output impedance is much lower than its input impedance. If a voltage gain greater than one is required we can use the following filter circuit.

Active Low Pass Filter with Amplification



$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

Gain of a first-order low pass filter

$$Voltage\ Gain,\ (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

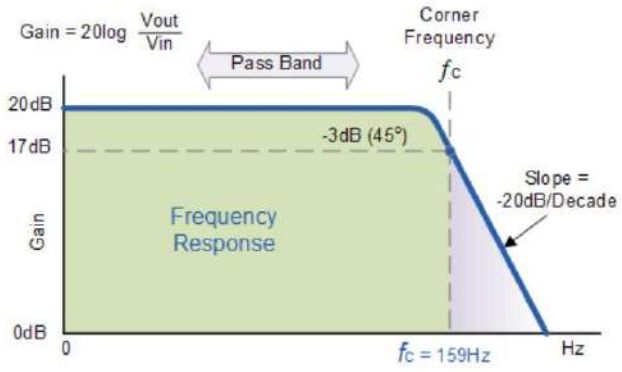
Where:

A_F = the pass band gain of the filter, (1 + R2/R1)

f = the frequency of the input signal in Hertz, (Hz)

fc = the cut-off frequency in Hertz, (Hz)

Frequency Response Curve



Multiple Feedback (MFB) Bandpass Filters:

- Bandpass Filter has Center frq and Bandwidth

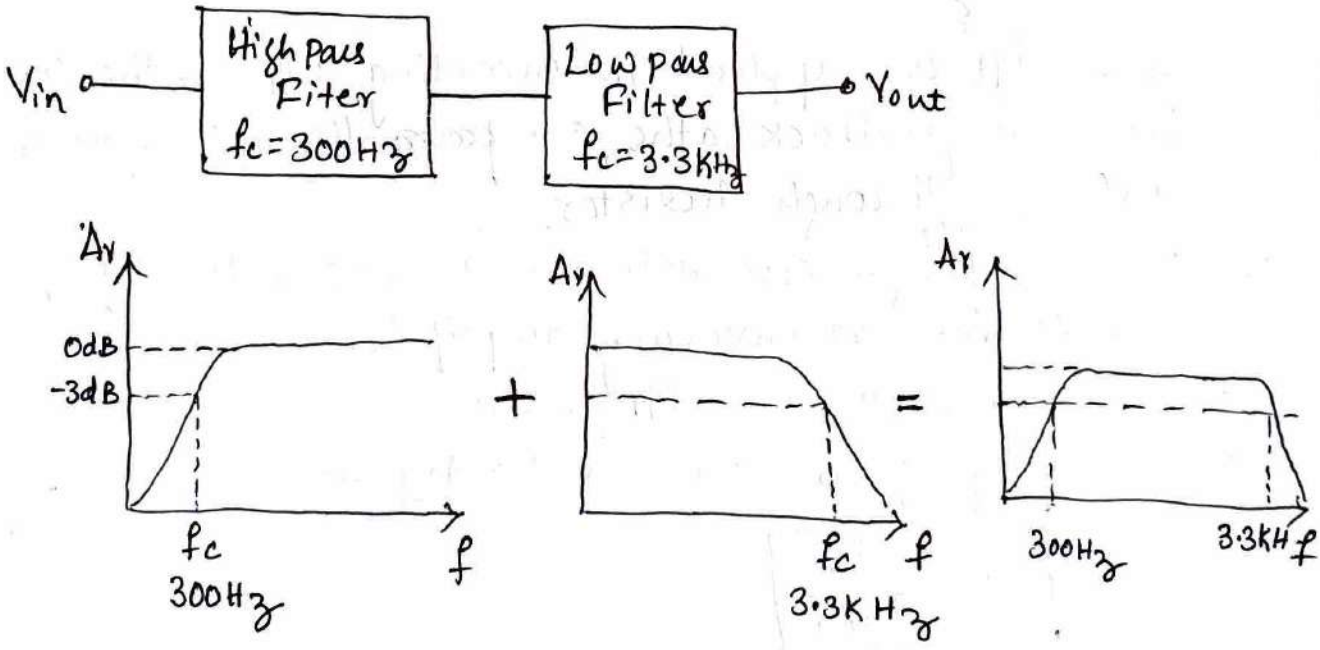
$$BW = f_2 - f_1$$

$$f_0 = \sqrt{f_1 f_2}$$

$$Q = \frac{f_0}{BW}$$

- when $Q < 1$ then Filter has wide band response and when $Q > 1$ the Filter has narrow response.
- The bandpass Filter are designed by cascading a LPF stage & a HPF stage *(for $Q < 1$)*

Wideband Fiters :-



- If we want to build a Bandpass Filter with lower Cut off Frq 300Hz & upper Cut off frq of 3.3KHz.
- Then the Center frq $f_0 = \sqrt{f_1 f_2} = \sqrt{(300)(3.3K)} = 995 Hz$
- Bandwidth $BW = f_2 - f_1 = 3.3K - 300 = 3KHz$
- $Q = \frac{f_0}{BW} = \frac{995}{3K} = 0.332$

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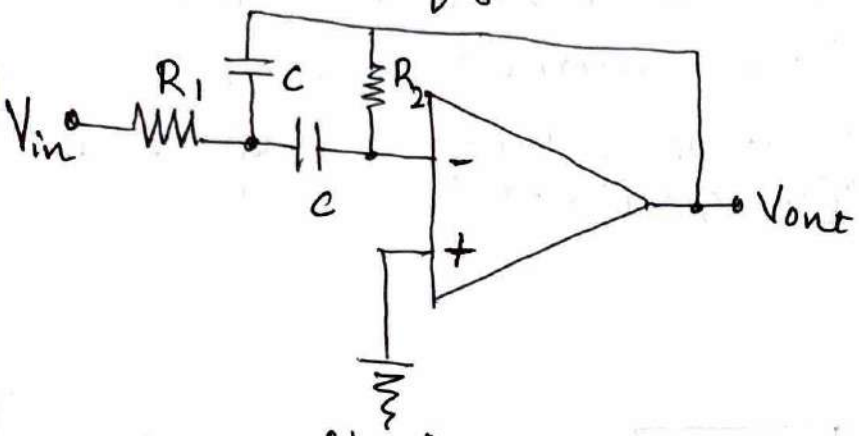
- The HPF has $f_c = 300Hz$ & LPF has $f_c = 3.3kHz$.
- When two decibles response are added we will get a BPF response with cut off frquencies of 300 Hz & 3.3KHz
- When $Q < 1$ we will use Cascade approach.

Narrow band Filters

- When $Q > 1$, we can use multiple Feedback (MFB) Filter as shown in fig. below



- Here i/p is applied to inverting i/p & the circuit has two feedback paths, one through capacitor & another through resistor.
- For the band of frequencies between low frq & High frq the Circuit acts as inverting amplifier.
- For other frquencies o/p is zero.
- The Voltage gain at the Center frq is

$$A_V = \frac{-R_2}{2R_1}$$

- The Q of the Circuit is

$$Q = 0.5\sqrt{\frac{R_2}{R_1}} \quad \text{(or)} \quad Q = 0.707\sqrt{-A_V}$$

- The Center frq is $f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$

$\because C_1 = C_2$

$$f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}}$$

Negative Feedback: Module-4

- In feedback network, Amplifier & Feedback are connected along with i/p signal to obtain o/p.
- difference b/w Feedback n/w & oscillator is that, in oscillator no i/p is given but in feedback n/w i/p is given.

- Two types of Feedback n/w
  - → Positive Feedback n/w: i/p signal & part of o/p signal are in phase.
  - → Negative Feedback n/w: i/p signal & part of o/p signal are out of phase.

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Types of Negative Feedback:

Input	o/p	Circuit	Zin	Zout	Converts	Ratio	Symbol	Type of amplifier
V	V	VCVS	∞	0	-	V_{out}/V_{in}	A_v	Voltage Amplifier
I	V	ICVS	0	0	i to V	V_{out}/i_{in}	r_m	Transresistance Amplifier
V	I	VCIS	∞	∞	V to i	i_{out}/V_{in}	g_m	Transconductance Amplifier
I	I	ICIS	0	∞	-	i_{out}/i_{in}	A_i	Current Amplifier

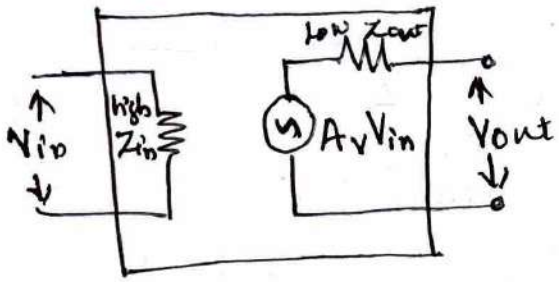
- I/p to negative feedback can be either a Voltage (or) a Current
- o/p signal can be either a voltage (or) a Current.
- There are 4 types of negative feedback.
- In VCVS (Voltage Controlled Voltage Source), i/p is voltage & o/p is also voltage, it has Stabilized gain, infinate i/p impedence & Zero o/p impedence & it is known as Voltage Amplifier.
- In ICVS (Current Controlled Voltage Source), i/p is current & o/p is voltage, here i/p impedence & o/p impedence is zero, it is known as Transresistance Amplifier

- In VCIS (Voltage Controlled Current Source) the i/p is Voltage & o/p is current, here i/p impedence & o/p impedence are infinate, it is known as Transconductance Amplifier.

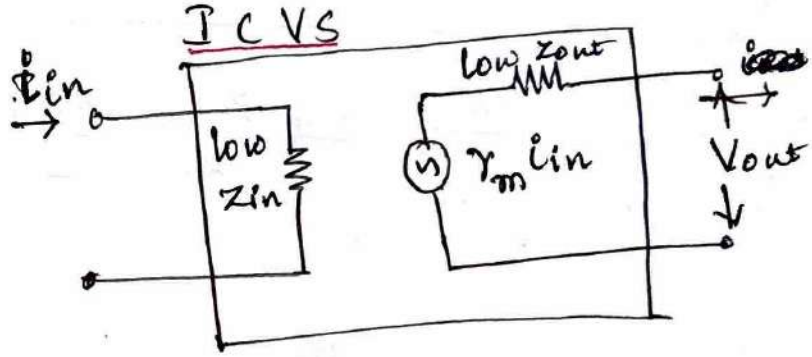
- In ICIS (Current Controlled Current Source), the i/p is Current & o/p is also current, here i/p impedence is '0' and o/p impedence is '∞'. It is known as Current Amplifier.

- ICVS converts Current to Voltage and VCIS converts Voltage to Current.

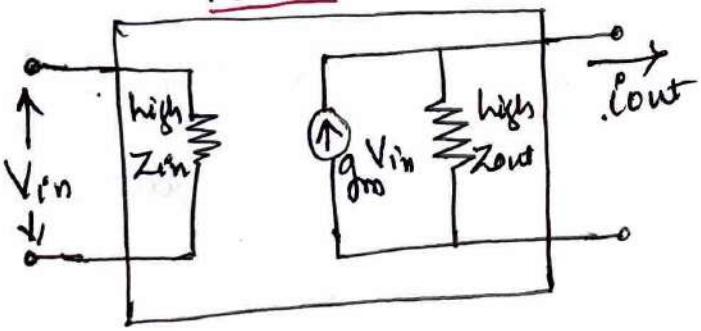
VCVS



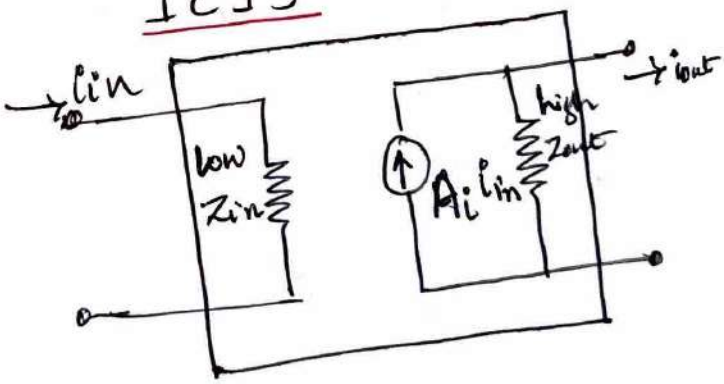
ICVS



VCIS



ICIS

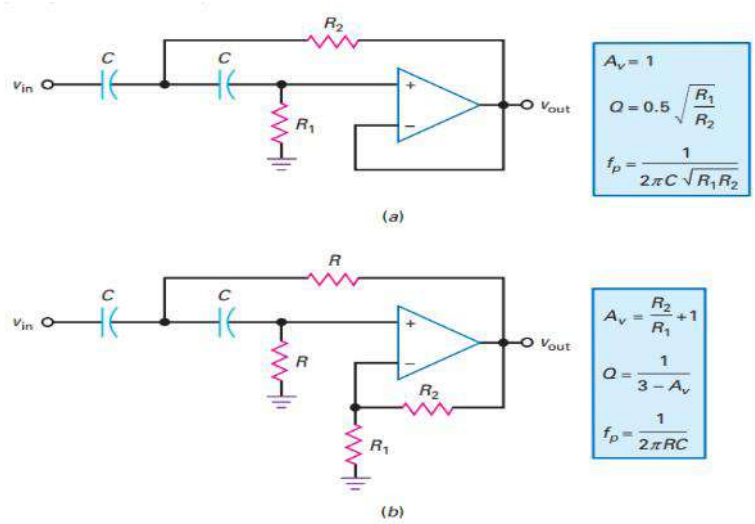


Second-Order High-Pass Filter

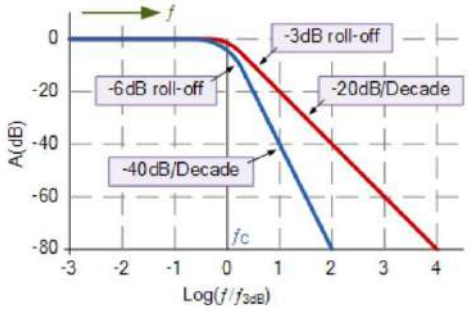
A **second-order high-pass filter** allows high-frequency signals to pass while attenuating low-frequency signals. Being "second-order" means it has a roll-off rate of 40 dB/decade) in the stopband, which is steeper than a first-order filter.

Circuit Diagram

A second-order high-pass filter can be implemented using two reactive components (capacitors) and two resistors. The most common configuration uses an **active filter design** with an operational amplifier (op-amp) to improve performance.



Frequency Response



Most designs of second order filters are generally named after their inventor with the most common filter types being: *Butterworth*, *Chebyshev*, *Bessel* and *Sallen-Key*. The Sallen-Key filter design is one of the most widely known and popular 2nd order filter designs, requiring only a single operational amplifier for the gain control and four passive RC components to accomplish the tuning.

Load Line Analysis

Load line analysis is a graphical method used in electronics to study the interaction between a circuit (typically involving a transistor or diode) and its connected load. The load line represents all possible operating points of the circuit under given conditions. There are two types of load lines:

1. **DC Load Line**: Represents the constraints imposed by the power supply and resistive load.
2. **AC Load Line**: Represents the constraints during small-signal operation, considering the impedance of the circuit.

---

1. DC Load Line

The **DC load line** shows the relationship between the output current and voltage of a device, based on the external DC circuit connected to it.

Derivation:

Using Kirchhoff's Voltage Law (KVL), consider a simple circuit with a transistor (or diode), a supply voltage (V_{CC}), and a load resistor (R_L):

$$V_{CC} = I_C R_L + V_{CE}$$

Where:

- V_{CC}: Supply voltage
- I_C: Collector current
- V_{CE}: Voltage across the transistor
- R_L: Load resistance

Rearranging for I_C:

$$I_C = \frac{V_{CC} - V_{CE}}{R_L}$$

Equation of the DC Load Line:

$$V_{CE} + I_C R_L = V_{CC}$$

This equation represents a straight line on the I_C-V_{CE} plane.

- Intercepts:
  - When $I_C = 0$: $V_{CE} = V_{CC}$ (x-axis intercept).
  - When $V_{CE} = 0$: $I_C = \frac{V_{CC}}{R_L}$ (y-axis intercept).

Significance:

The DC load line provides all possible operating points for the device under steady-state conditions.

2. AC Load Line

The **AC load line** is used to analyze small-signal behavior. It considers the dynamic impedance (r_L) of the circuit during signal operation.

Derivation:

In small-signal analysis, the impedance r_L replaces R_L, and the voltage-current relationship during AC operation is given by:

$$v_{ce} + i_c r_L = V_{CE(Q)}$$

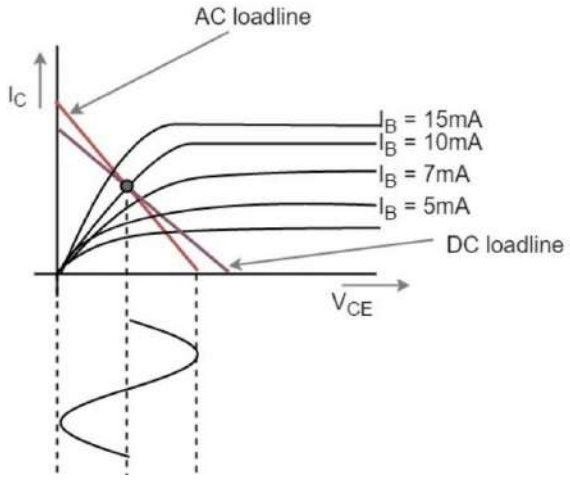
Where:

- v_{ce}: AC voltage across the transistor
- i_c: Small-signal current
- $V_{CE(Q)}$: Quiescent point (Q-point) voltage

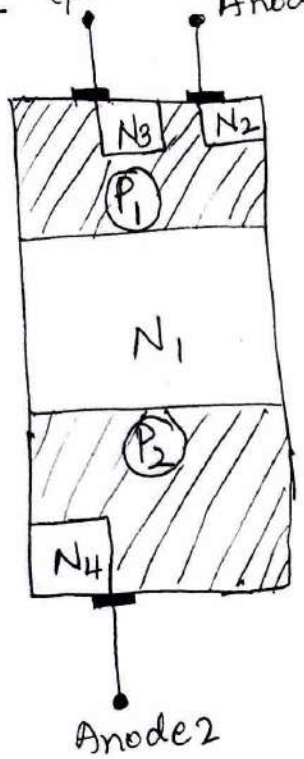
AC Load Line Equation:

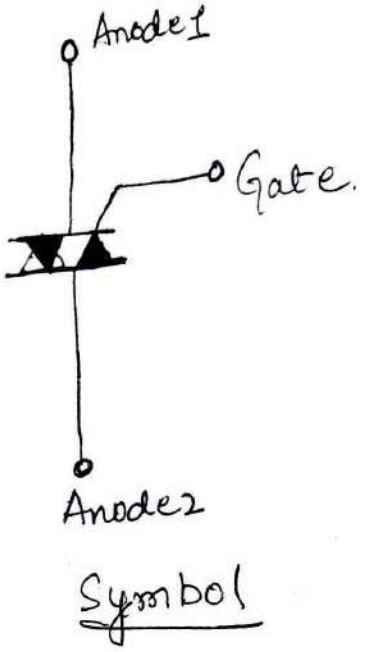
$$v_{ce} = V_{CE(Q)} - i_c r_L$$

This line has a slope of $-1/r_L$ and passes through the Q-point. It is steeper than the DC load line if $r_L < R_L$.



TRIAC: Bidirectional Thyristors.





Symbol

→ TRIAC is a bidirectional device.

→ It Can conduct in both Forward bias and Rever bias Conditions.

→ 'TRI' indicates 3 terminals

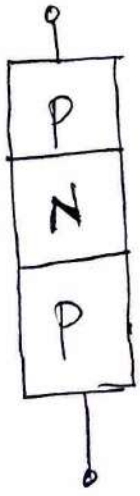
→ 'AC' indicates alternating current.

Applications:-

(i) Used as high power Lamp Switch

(ii) To Control a C power to the load.

DIAC:



Symbol

→ It conducts in both Forward and Reverse bias Condition.

→ Two terminal device with three Semiconducting layers.

→ 'D' indicates two terminals.

→ AC indicates Alternating current.

Application :-

(i) It can be used as lamp dimmer.

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IGBTs

(Insulated Gate bipolar Transistor)

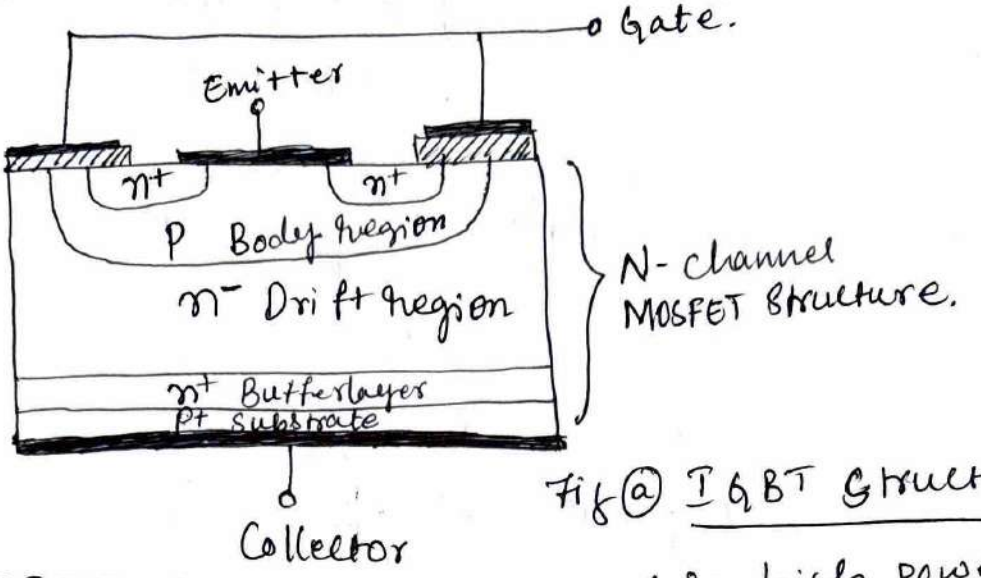
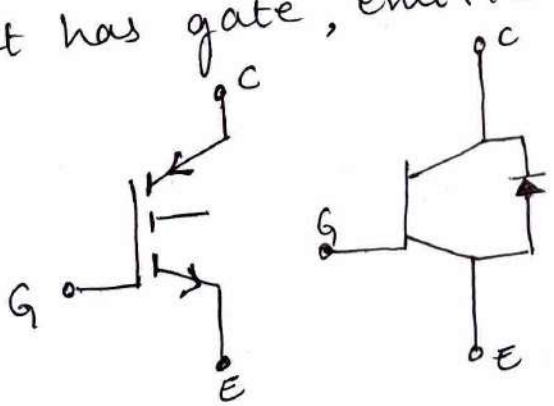
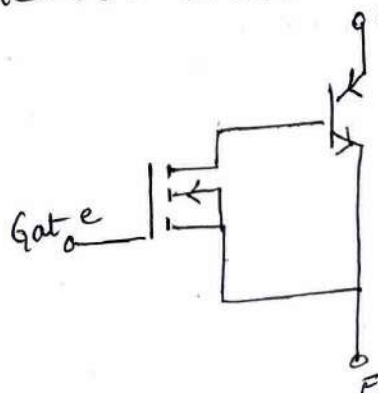


Fig (a) IGBT Structure

- Power MOSFET & BJTs can be used in high power switching application.
- The MOSFET has advantage of greater switching speed & BJT has lower conduction losses.
- By combining the lower conduction loss of a BJT with switching speed of Power MOSFET, we can have an Ideal device
- This hybrid device is known as IGBT.
- It's structure is shown in fig (a)
- Its structure resembles an n-channel power MOSFET constructed on a P-type substrate.
- It has gate, emitter & Collector terminals



(b) Symbol of IGBT

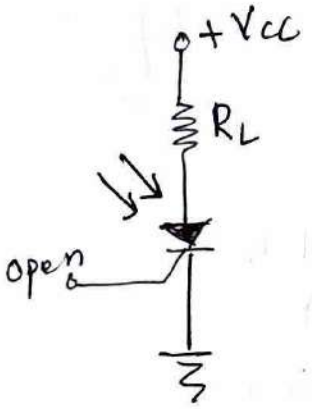


(c) Simplified Circuit

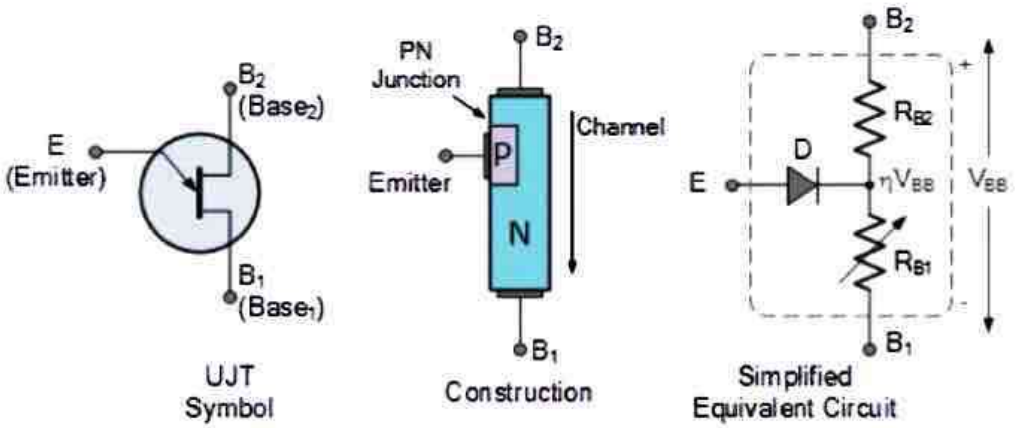
- Two versions of device are reffered as punch Through (PT) & non punch Through (NPT) IGBTs
- punch through (PT) IGBT has an n^+ buffer layer b/w p^+ & n^- region.
- NPT IGBT has no n^+ buffer layer.
- fig © shows an equivelent circuit of IGBT
- Input control is Vtg b/w Gate & Emitter & Output is Current b/w Collector & Emitter.

other Thyristors

(i) photo-SCR



- It is also known as light activated SCR.
- The arrow represents incoming light that passes through a window & hits the depletion layer
- then the valance electrons dislodge from their location & become free electrons.
- free electrons Starts positive feedback and SCR Closes.
- After light trigger has Closed, the SCR still remain closed.
- For maximum Sensitivity to light, Gate is left open.



Unijunction Transistor

The UJT is a three-terminal, semiconductor device which exhibits negative resistance and switching characteristics for use as a relaxation oscillator in phase control applications

The **Unijunction Transistor** or **UJT** for short, is another solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triac's for AC power control type applications.

Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.

Although the *Unijunction Transistor* has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can not be used to amplify a signal but instead is used as a ON-OFF switching transistor. UJT's have unidirectional conductivity and negative impedance characteristics acting more like a variable voltage divider during breakdown.

Like N-channel FET's, the UJT consists of a single solid piece of N-type semiconductor material forming the main current carrying channel with its two outer connections marked as *Base 2* (B_2) and *Base 1* (B_1). The third connection, confusingly marked as the *Emitter* (E) is located along the channel. The emitter terminal is

represented by an arrow pointing from the P-type emitter to the N-type base.

The Emitter rectifying p-n junction of the unijunction transistor is formed by fusing the P-type material into the N-type silicon channel. However, P-channel UJT's with an N-type Emitter terminal are also available but these are little used.

The Emitter junction is positioned along the channel so that it is closer to terminal B_2 than B_1. An arrow is used in the UJT symbol which points towards the base indicating that the Emitter terminal is positive and the silicon bar is negative material. Below shows the symbol, construction, and equivalent circuit of the UJT.

3.7 THE PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT)

The PUT is an improved version of a UJT. Actually, the PUT is a *PNPN* device, but its operation is so similar to the UJT that it is always considered with the UJT. As we shall see, the PUT behave like a UJT whose trigger voltage V_p can be set by the circuit designer via an external voltage divider.

Figure 3.25 shows the *PNPN* structure and the circuit symbol for the PUT. The anode (A) and cathode (K) are the same as for any *PNPN* device. The gate (G) is connected to the *N*-region next to the anode. Thus, the anode and gate constitute a *P-N* junction. It is this *P-N* junction which controls the "on" and "off" states of the PUT. The gate is usually positively biased relative to the cathode by a certain amount, V_g. When the anode voltage is less than V_g, the anode-gate junction is reverse-biased and the *PNPN* device is in the "off" state, acting as an open-switch between anode and cathode. When the anode voltage exceeds V_g by about 0.5 V, the anode gate junction conducts, causing the *PNPN* device to turn "on" in the same manner as does forward biasing the gate cathode junction of an SCR. In the "on" state, the PUT acts like any *PNPN* device between anode and cathode (low resistance and $V_{AK} \approx 1$V). The PUT is also referred to as a complementary SCR (CSCR).

The normal bias arrangement for the PUT is shown in Fig. 3.26. The voltage divider, R_1 and R_2 sets the voltage at the gate V_g. Note that R_1 and R_2 are external to the device and can therefore be chosen to produce any desired value of V_g. The anode cathode bias is provided by E_{dc}. As long as $E_{dc} < V_g$, the device is "off" with $I_A = 0$ and all of E_{dc} present across the anode cathode ($V_{AK} = E_{dc}$). The "off" state is summarized in part (a) of the figure.

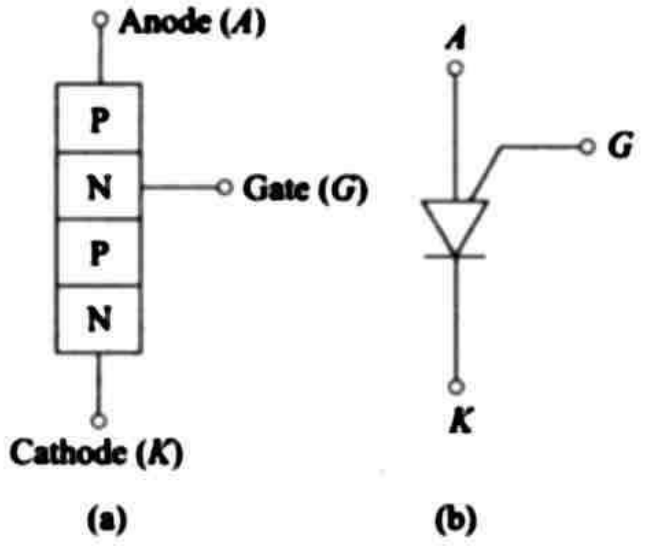


Fig. 3.25 *(a) PUT structure (b) circuit symbol*

If E_{dc} is increased to about 0.5V greater than the V_g bias value, the device turns "on". In other words, the peak-point voltage V_p for the PUT is given by

$$V_p = V_g = 0.5 \text{ V} \tag{3.19}$$

In the "on" state, the anode–cathode voltage, V_{AK}, drops to ≈ 1V and the anode current, I_A, is essentially equal to E_{dc}/R_1 being limited by R. In addition, V_g drops to a very low value (≈ 0.5 V) since R_2 is now shunted by the "on" *PNPN* structure. The PUT will remains in the "on"-state until the anode current is decreased below the valley-current, I_v. The "on" state is summarized in part (b) of the figure.