USN | | | | | | | | | | |

INTERNAL ASSESSMENT TEST – I

Sub:	VLSI Design and Testing							Code:	BEC602
Date:	26/ 03 / 2025	Duration:	90 mins	Max Marks:	50	Sem:	VI	Branch:	ECE

Answer any 5 full questions

		Marks	CO	RBT
1	What is the role of a transmission gate in CMOS circuits? Explain its operation using both NMOS and PMOS transistors. Discuss the advantages of using CMOS transmission gates over single NMOS or PMOS switches.	[10]	CO1	L1
2	Realize the following logic expression using CMOS: (i) $Y = A + BC$ (ii) $Y = \overline{A + BC}$	[5+5]	CO1	L3
3	Write a note on Additional CMOS Circuit: Pseudo NMOS, Cascaded NMOS and Tristate inverter	[5+5]	CO2	L2

4	Explain the CMOS inverter transfer characteristics highlighting the region of operation of the MOS transistors.	[10]	CO2	L1
5	Explain the operation of an n-channel enhancement mode MOSFET with neat diagrams for different conditions of V_{DS} & V_{GS}.	[6+4]	CO2	L2
6	Explain the following: (a) Threshold Voltage (b) Channel length modulation (c) Body Effect	[10]	CO2	L1
7	Compare CMOS and NMOS Technology.	[10]	CO1	L1

CI

M.S. Ananth Kumar
CCI

HOD

2. ९. $Y = A + BC$

Here the OR (+) operation is taking plac.

> For Nmos we need to draw in parallel.

> For pmos we need to draw in Series.

Here AND (.) operation is also taking plac so we need to use

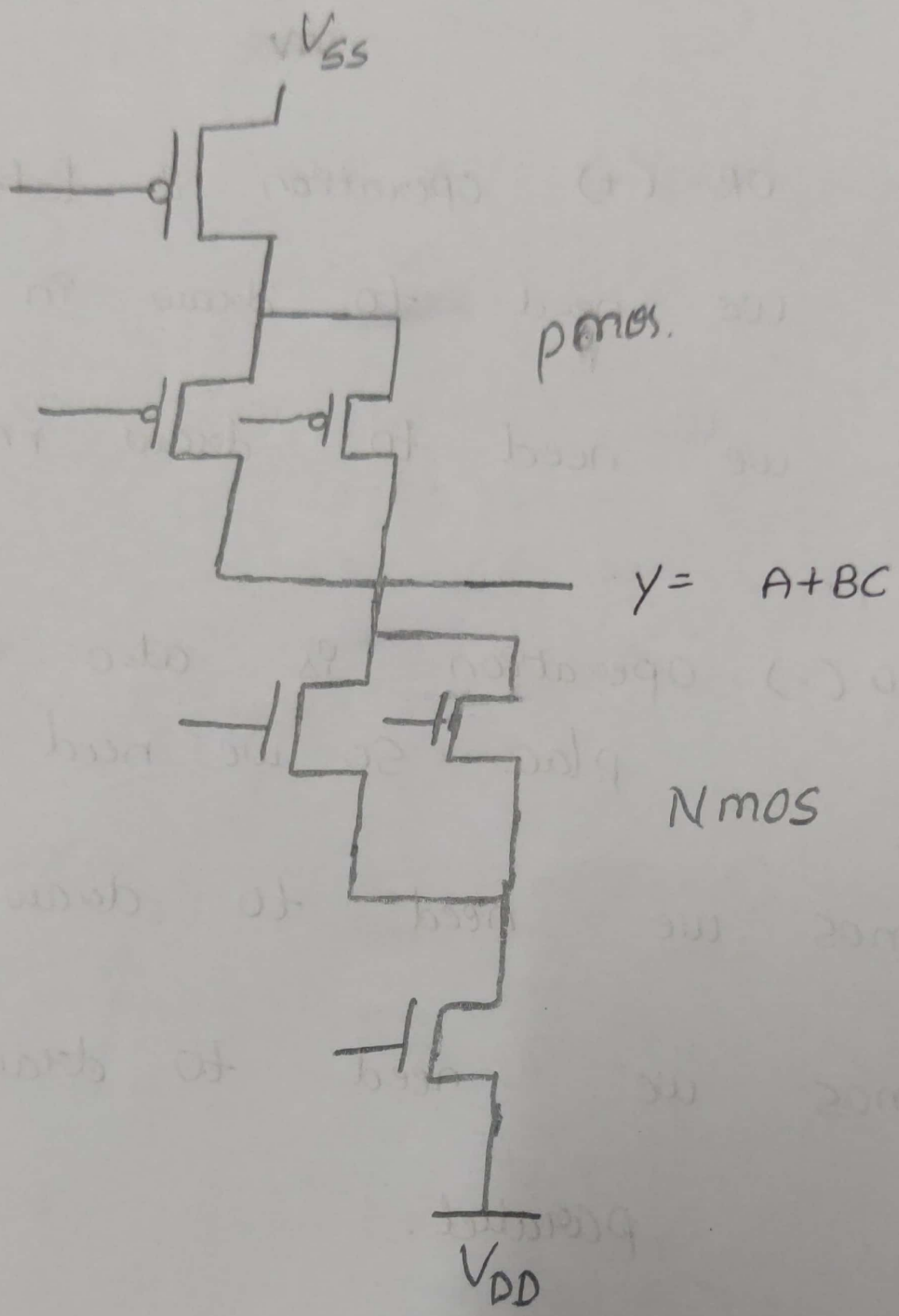
> For Nmos we need to draw in Series

> For pmos we need to draw in parallel.

CMOS Circuit

> Nmos we need to drawn B and C in Series with A in parallel.

> pMos we need to draw B and C in parallel with A in Series.


V_{SS}
pmos.
y= A+BC
Nmos
V_{DD}

Q11. $Y = \overline{A + BC}$

Here the OR (+) operation is taking place.

> For NMOS we need to drawn in parallel.

> For pMOS we need to drawn in Series.

Here the AND (·) operation is taking place.

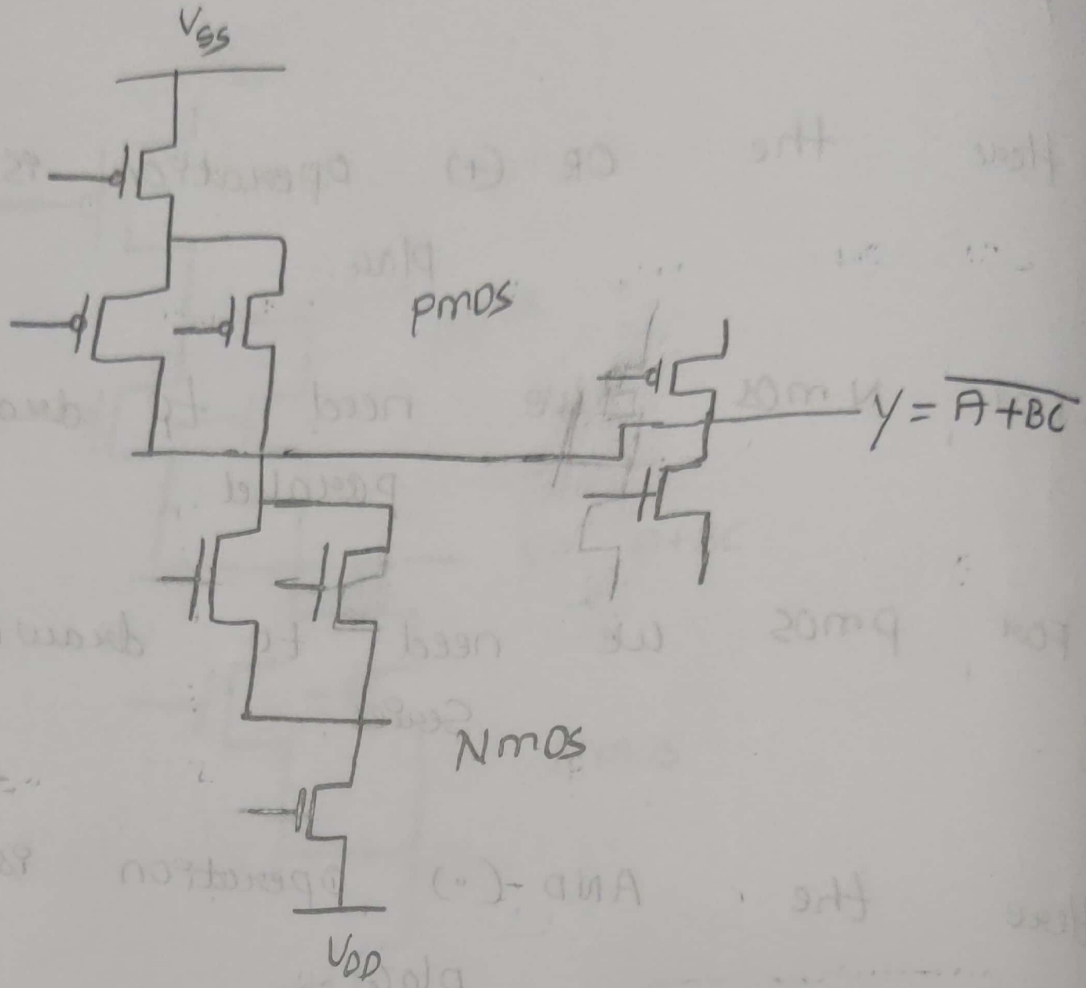
> For NMOS we need to drawn in Series.

> For pMOS we need to drawn in parallel.

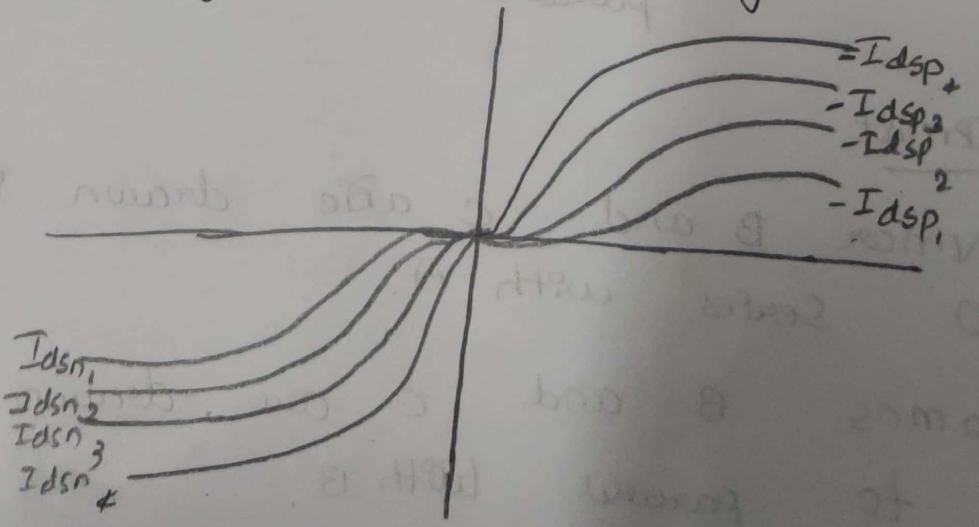
CMOS Circuit

> For Nmos B and C are drawn in parallel to Series with A.

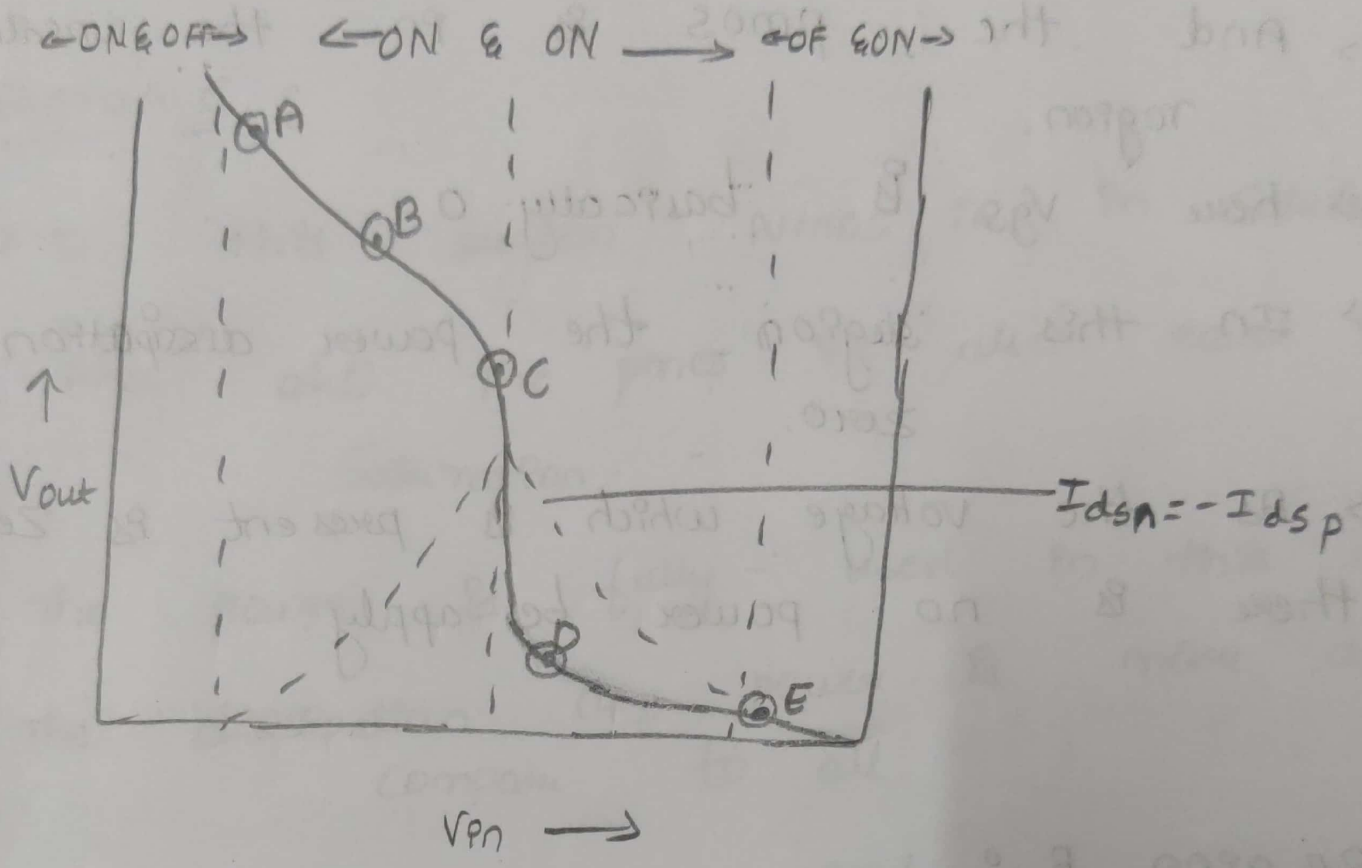
> For pmos B and C are drawn in Series to parallel with B.



4. Coms characteristic can be told by adding the pmos and N mos transfer characteus together.



The region of operation of the MOS transistor based on this.



There are basically 4 regions are there namely A, B, C, and E.

among those regions let us discuss about one by one.

Region A.

> In this region N mos is OFF
> And the pmos is on the unsaturated region.
> here Vgs is basically 0.
> In this region the power dessipation is zero.
> As the voltage which is present is zero there is no power be apply.

Region B :

> In this region N mos is Saturated
> And the pmos is on ohmic situation.
> Here $V_{in} = V_{tn}$, on the region the Vout we can found out.
> In this region power dessipation is no more zero.

The equation of Vout can be given by

$$V_{out} = (V_{in} - V_{tp}) - \sqrt{(V_{in} - V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)(V_{in} - V_{tn})}$$

Region C :

> In this region Nmos is in Saturated.

> And also the pmos is also equal to Saturation.

> The power is fully used in this region

> The dessipation of power is more as compare to all.

> The output Vout which reaches maximum in this region. Current can be given by

$$I_{dsn} = \frac{B_n}{B_p}(V_{in} - V_{tp})^2$$

$$I_{dsp} = -\frac{B_n}{B_p}(V_{in} - V_{dd} - V_{tn})^2$$

Region D :

> In this region Nmos is Ohmic

> And the pmos is in Saturated.

> It is just the inverted version of B region.

> The power consumption is less as compared.

> The Conduction of current can be given by.

$$I_{dsp} = \frac{1}{2}\frac{\beta_n}{\beta_p}\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)^2$$

$$I_{dsn} = -\frac{1}{2}\frac{\beta_n}{\beta_p}\left(V_{in} - V_{tp}\right)^2$$

Region E

> In this region NMOS is saturated

> And pmos is in OFF condition.

> Here there is no power consumption

> There is no peak value.

> Here the value of Vout = Zero.

> There is no conduction of current.

5. N- channel MOSFET in which it consists of electrons.

- when the voltage which is applied to the gate and source then the electrons are attracted towards the source of gate and has depels mode.

. It consist of a gate, source and drain.

. It is a sandwich of p substrate, metal layer and insulation layer.

. It is most effecent switch.

. usually MOSFET is always a open switch.

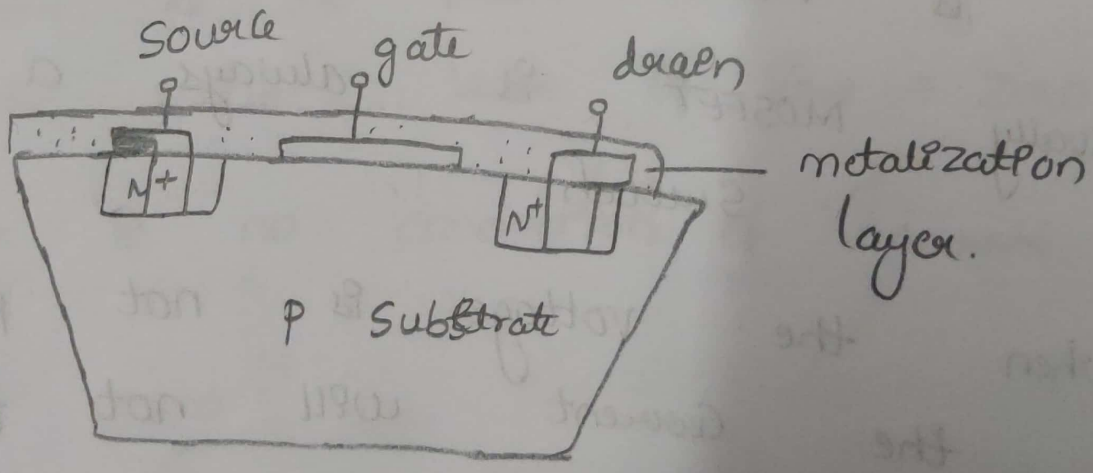
. when the voltage is not positive then the current will not flow from source to gate so there is no conduction take place.

> For conduction they need to provide some maximum voltage which is called as the threshold voltage. (V_t).

> If current needs to move then we need to apply threshold voltage.

> When the voltage which is given to the gate of the sour then it will provide an electric field so that it can attract the electrons just below the gate.

> And they also repels it.



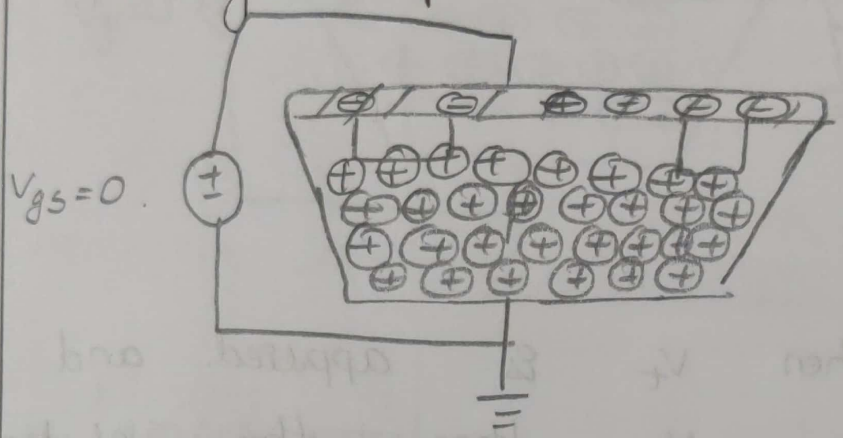
> When the threshold voltage is increased the p type will be changed to n type.

It consists of 3 modes

1. Accumulation.

> In this $V_{gs} = 0$.

> when the voltage which is provided for the gate then there is no exchange of electrons takes.



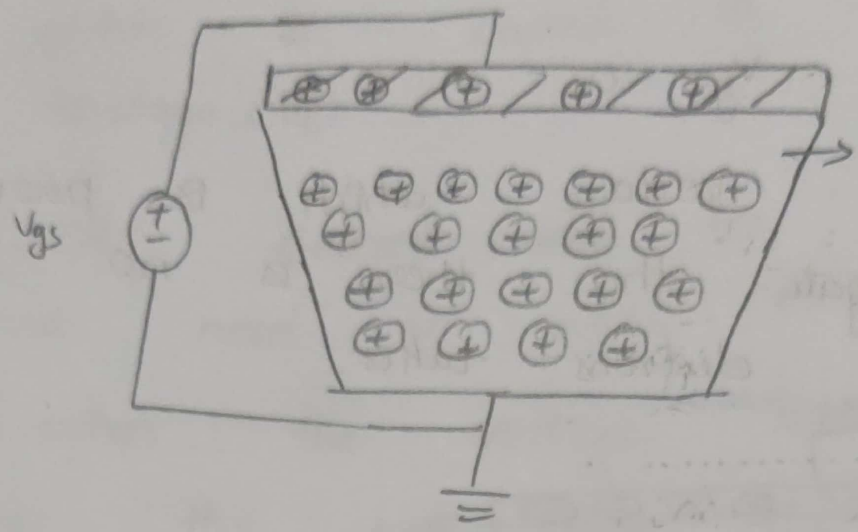
2. Depletion.

> In this region the voltage is provided to gate then the electrons which will came under the gate.

> The holes which will repels and they came under the gate

> There is no conduction between source and drain.

> That region which is formed is known as depletion region.

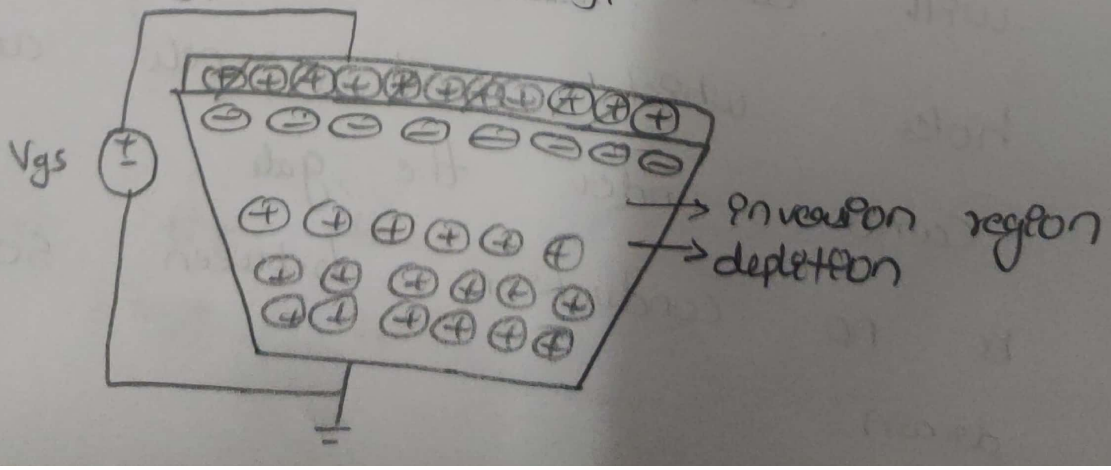


3. Inversion mode

> In this when V_t is applied and it has more V_t then the electron are move towards to subtrate.

> The holes which will repel will came under the gate

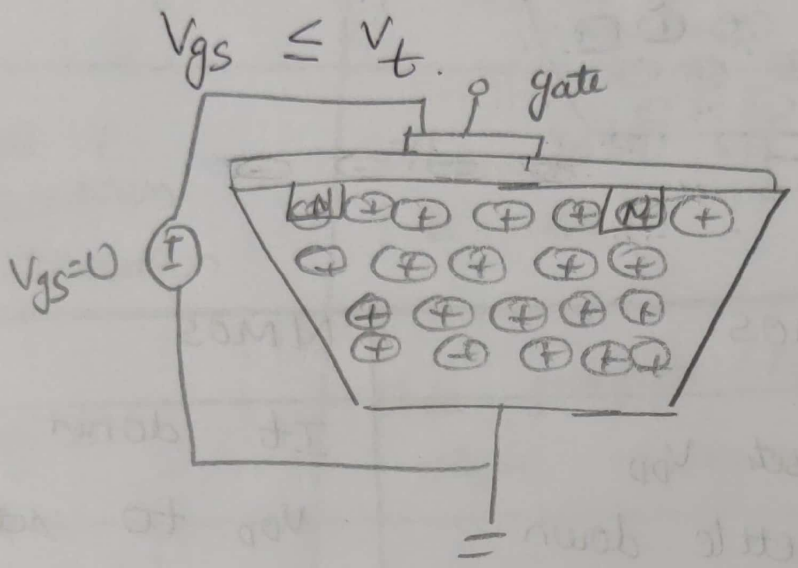
> This will make in inversion of P type to n type.



Conditions of V_{DS} & V_{GS} depends on.

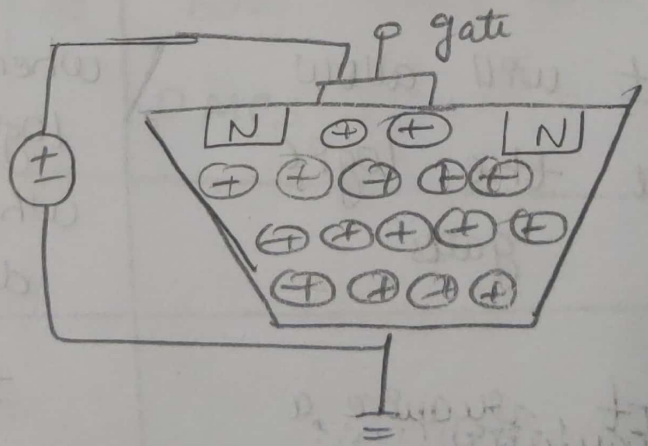
zero state
Unsaturated
Saturated

1. In this state the $V_{gs} = 0$.



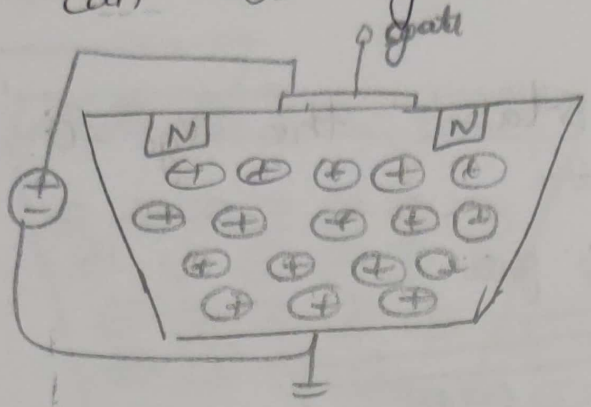
2. Unsaturated

It can be given by $V_{dd} < V_{gs} - V_t < V_{sd}$



Saturated

It can be given by $V_{dd} < V_{gd} < V_{gg} - V_t$



7.

Feature	CMOS	NMOS
logic levels	It sets V_{DD} to settle down	It do not sets V_{DD} to settle d
Transition time	Rise time and fall time in same order	Rise time is quite slow than fall time.
Transmission gate	It will allow all the logic gates	when it is zero logic it will allow when it '1' it is discarded
Power Supply	It require a more power supply of 1.5V - 2.5V	It does not regire more power.

7.			
	power dissipation	It has no power dissipation	It has more power dissipation
	prepating	It will make the V_{DD} and V_{gs} a logic value	It will not going to do it
	pull up pull down Operation	The ratio of this is 2:1	They usually show logic 0
	layout	This preffer regular style design	It preffer normal layout
	Effiency	COMS is more compare to Nmos	NMOS is more effecent
	combination	It is the combination of both NMOS and PMOS	It consist of electrons.

6. a. Threshold Voltage

> We all known the the maximum voltage which has to be given to the channel which is called as the threshold voltage.

> The threshold voltage can be represented by V_t.

> when an channel in which V_t is increased then it will allow the conduction.

> This threshold voltage which consist of some component.

> gate voltage
> gate metal layer.
> gate insulator.
> dopping
> Interface on the N type silicon
> Insulation layer.

> The threshold voltage which plays an important role in the increasing the conduction of a channel.

> It will helps the movement of electrons

b. Channel length modulation

> It is used to reduce the length and to make it shorter.

> The inversion which is the light should to make in the shorter way.

> The current which is present in it which needs to to make flow in a speed rate.

> when we provide V_t the movement of electrons takes place means the current which is present in it got speed up.

> The current is inversly proportional to the length.

> As the length and current which are inversely proportional to each other.

> when we are going to provide and high rate of current so that the length will be decreased.

> As the current which is flowing is a faster rate the length also become short

- So in order to achieve the Channel length modulation we need to increase the speed of current so that it will length will be Shortened.

- These are all Second order modes:

iii.

Body effect

> It is basically related to the increase in the V_{SB} which is called of as substrate bias voltage

> As there is an increase in the V_{SB} there is also an increase in the threshold voltage.

> V_{SB} and V_t are directly proportional to each other.

> As soon as the V_{SB} increases V_t will also be increased.

> when the substrate bias voltage is more then we are going to get the V_t also increased.

> Main aim is to increase the Substrate bias voltage.