

CBCS SCHEME

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21CS34

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Outline the basic operational concepts of processor with neat diagram. (08 Marks)
- b. Explain Big-Endian and Little-Endian byte and word addressing with an example. (08 Marks)
- c. Evaluate $(A) + (B) * (C) + D$ using one address instruction. (04 Marks)

OR

- 2 a. Write note on :
 - i) Byte addressability
 - ii) Condition codes
 - iii) Single bus structure. (08 Marks)
- b. List different addressing modes. With neat figure and an example, explain indirection and pointers addressing mode. (08 Marks)
- c. Discuss the basic performance equation and ways to achieve high performance. (04 Marks)

Module-2

- 3 a. What is bus arbitration? Explain distributed arbitration scheme. (08 Marks)
- b. With neat timing diagram, explain an input transfer using multiple clock cycles in synchronous bus. (08 Marks)
- c. With supporting figure, explain interrupt nesting. (04 Marks)

OR

- 4 a. How would you organize hardware interrupt to implement a common interrupt request line? (08 Marks)
- b. With neat diagram, explain a general 8 bit parallel interface circuit. (08 Marks)
- c. What are exceptions? List and explain different types of exceptions. (04 Marks)

Module-3

- 5 a. With neat diagram, explain organization of bit cells in a memory chip consisting of 16 words of 8 bits each. (08 Marks)
- b. Explain the internal structure of synchronous DRAM. (08 Marks)
- c. Explain the following:
 - i) Memory Bandwidth
 - ii) Memory Latency (04 Marks)

OR

- 6 a. Explain internal organization of a 16 Megabit DRAM chip configured as $2M \times 8$ cells. (08 Marks)
 b. What is memory mapping? Explain set-associate mapping. (08 Marks)
 c. Explain the following: i) ROM ii) EPROM (04 Marks)

Module-4

- 7 a. Perform the following using 2's complement :
 i) $(+2) + (+3)$
 ii) $(+7) + (-3)$
 iii) $(+7) - (-7)$
 iv) $(+6) - (-7)$ (08 Marks)
 b. With neat diagram, explain register transfers. (08 Marks)
 c. Describe array implementation for multiplication of positive numbers. (04 Marks)

OR

- 8 a. Explain in detail, organization of control unit. (08 Marks)
 b. With neat diagram, explain 4-bit-carry look ahead adder. (08 Marks)
 c. With neat sketch, explain the organization of micro programmed control unit. (04 Marks)

Module-5

- 9 a. Explain parallel processing, with neat diagram. (10 Marks)
 b. Explain Single Instruction Stream Multiple Data (SIMD) array processor. (10 Marks)

OR

- 10 a. Explain basic idea of instruction pipe line. (10 Marks)
 b. Write note on memory interleaving. (10 Marks)
